AOC Service Manual
A42W64AT4

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1、 SPECIFICATION

1-1 General Specification

Item		Specification		
Panel Spec	Screen size	42 inch plasma display panel		
	Aspect	16:9		
	Display pixels	852 x 480 (WVGA)		
	Effective display size	932mm x 532mm		
	Number of color	16.7 million colors		
	Contrast Ratio	10000:1 (in dark room)		
	Peak brightness	1500 cd/㎡		
TV Mode	TV Tuning	1 Tuners, Air:69 channels Cable:135 channels		
	Sound system	M		
	Color system	ATSC / NTSC		
Video Mode	AV1 (S_Video/Video)	Video RCA x 1	NTSC	Audio: L/R x 1
		S-Video1 x 1	NTSC	
	AV2 (S_Video/Video)	Video RCA x 1	NTSC	Audio: L/R x 1
		S-Video2 x 1	NTSC	
	AV3 / AV4 COMPONENT X 2 (YCbCr/YPbPr)	YCbCr/YPbPrx 2	480i	Audio: L/R x 2
			1080i	
			480P	
			720P	
PC Mode	Signal input	Analog：D-Sub 15 pin		
	Plug and play	DDC / 2B		
	Support Frequency	FH:31KHz to 80KHz ， FV:50Hz to 85Hz		
	D-Sub Mode	VESA: 640 x 480 VESA: 800 x 600 VESA: 1024 x 768 VESA: 1280 x 1024		
	D-Sub Audio	Earphone (3.5ø)		
DVI Mode	Signal input	Digital：DVI-D 24 pin		
	Plug and play	DDC / 2B		
	DVI Mode	720P 1080i 480P		
	DVI Audio	Earphone (3.5ø)		
Power	Power input sources	AC 100-240V , 50/60Hz		
	Power consumption	≤350W		
Environment	Operation Temperature	+ 0 °C ~ + 40 °C		
	Storage Temperature	- 10 °C ~ + 50 °C		
	Humidity	10% -- 85%		
Dimension	Width x Height x Thickness	1038 x 726.5 x 240 (mm)		
Net weight	With Stand	34Kg		
Accessory	Remote Control Transmitter, Battery X 2, Power Cord, User's Manual, RCA Cable, D-SUB Cable, DVI Cable.			

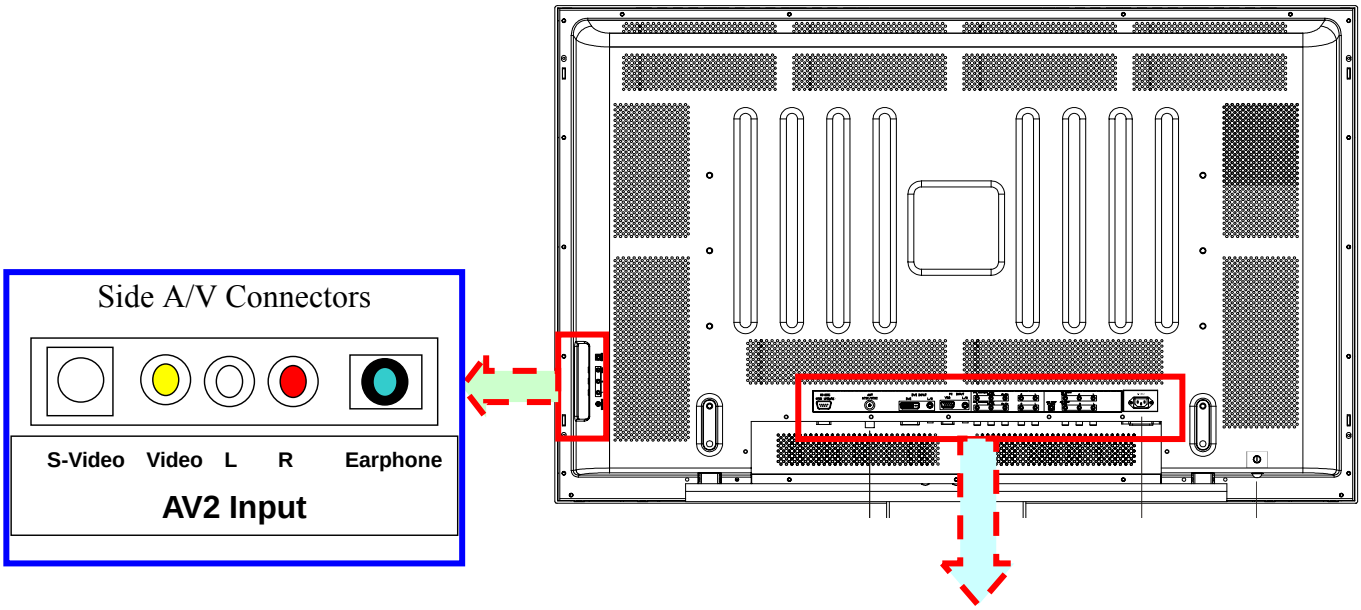
1-2 Feature Summary

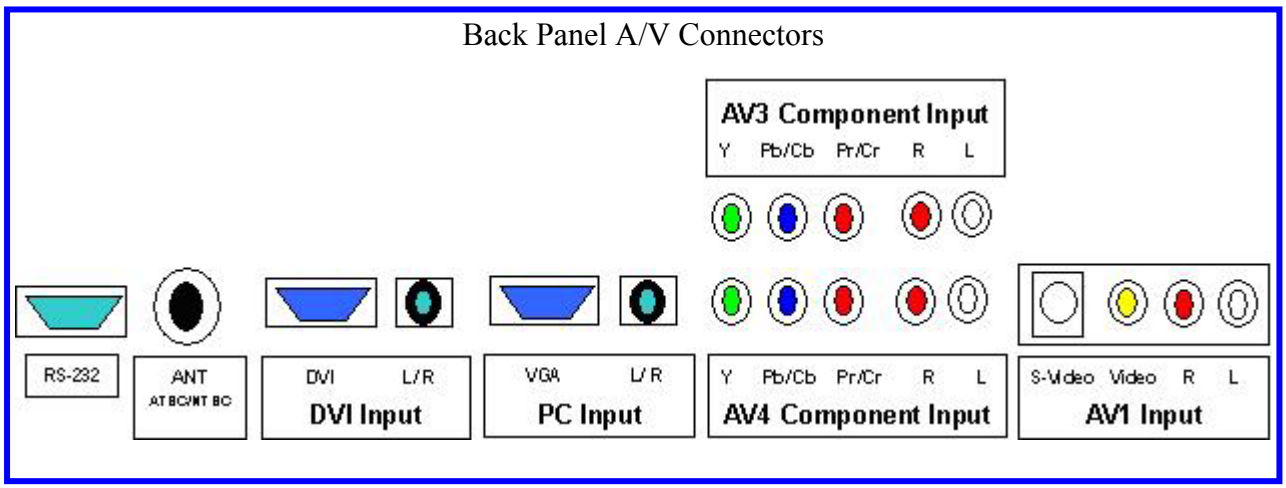
The following is the specification summary for the display:

- **107 cm (42”) 16:9 Large Screen Flat Panel Plasma Display**
- **Resolutions: WVGA 852 (H) X 480(V) pixels, (1 pixel = 1 R, G, B cells)**
- **1.095 mm (H) X 1.110mm(V) pixel pitch.**
- **Viewing Angle: 160° Vertically and Horizontally**
- **Internal TV Tuner, Air: 69 channels Cable: 135 channels**
- **Typical Maximum Contrast Ratio: 10000:1**
- **Typical Maximum Brightness: 1500 cd/m^2**
- **ATSC receiver, MPEG-2 decoder**
- **NTSC receiver, Video decoder**
- **Dual Video, Dual S-Video**
- **Dual Y Pb Pr (480i,480p,720p,1080i) HDTV Ready**
- **PC D-SUB 15Pin INPUT**
- **D-SUB analog video with rate 50Hz to 85 Hz vertical refresh rate and 31KHz to 80KHz horizontal frequency**
- **DVI-D Signal (TMDS) INPUT, Support HDTV, SDTV**
- **Closed Caption / V-chip**
- **Composite, S-Video, and component video receiver**
- **MIPS controller**
- **Auto Scan TV Channels**
- **Field upgradable firmware**
- **Universal Power Supply designed for worldwide application**
- **Operating power consumption less than 350 W**
- **Standby power consumption less than 1 W**

1-3 External interface

Most of these interfaces are located at the back-panel. There's also a group of connectors located on the side of this device for easier access. The following figures depict these A/V connectors.





1-3-1 Video/Audio Inputs

The following sections specify the video/audio inputs for A42W64AT4.

1-3-1-1 TV Antenna Interface

①. TV Antenna Connector

A42W64AT4 shall provide a F-type cable connector with 75 ohms termination on its back panel for reception of radio frequency signals.

②. TV Systems

A42W64AT4 shall be capable of receiving the following broadcasting systems in the North America region.

- Analog terrestrial and cable broadcasting in NTSC system and “M” sound system.
- All 18 formats specified for ATSC digital broadcasting
- Clear QAM digital cable broadcasting

③. TV Channel Coverage

The RF tuner shall be capable of covering 55.25 to 859.25 MHz and tuning to the following channels:

- VHF: channel 2 through 13
- UHF: channel 14 through 69
- Mid band cable: A1 through A8, A through I
- Super band cable: J through W
- Hyper band cable: AA through ZZ, AAA, BBB
- Ultra band cable: channel 65 through 94, 100 through 125

④. Closed Caption

A42W64AT4 shall support closed caption and text mode for both video and TV system. These supports shall include channel ½ and field ½ selectable features.

⑤. V-Chip

A42W64AT4 shall support MPAA grade for movie and TV Parental Guideline for TV. This support shall include changeable password.

1-3-1-2 AV1

A standard definition (SD) analog video/audio source designated as AV1 shall be located on its back panel. It comprises the following electrical connections. Only one of the two video inputs shall be connected.

①. S-Video Input

A42W64AT4 shall provide a 4-pin mini-DIN connector for connection to an external S-Video source.

②. CVBS Video Input

A42W64AT4 shall provide a RCA type receptacle for connection to an external CVBS source.

③. Audio Inputs

A42W64AT4 shall provide two RCA type receptacles for the stereo audio signal associated with AV1 input.

1-3-1-3 AV2

A standard definition analog video/audio source designated as AV2 shall be located at the side of A42W64AT4. It comprises the following electrical connections. Only one of the two video inputs shall be connected.

①. S-Video Input

A42W64AT4 shall provide a 4-pin mini-DIN connector for connection to an external S-Video source.

②. CVBS Video Input

A42W64AT4 shall provide a RCA type receptacle for connection to an external CVBS source.

③. Audio Inputs

A42W64AT4 shall provide two RCA type receptacles for the stereo audio signal associated with AV2 input.

1-3-1-4 AV3

A YPbPr/YcbCr type component video interface designated as AV3 shall be located on its back panel. It comprises the following electrical connections.

①. Video Inputs

A42W64AT4 shall provide three RCA type receptacles for connection to an external component video source.

②. Audio Inputs

A42W64AT4 shall provide two RCA type receptacles for the stereo audio signal associated with Component1 input.

1-3-1-5 AV4

A YPbPr/YcbCr type component video interface designated as AV4 shall be located on its back panel. It comprises the following electrical connections.

①. Video Inputs

A42W64AT4 shall provide three RCA type receptacles for connection to an external component video source.

②. Audio Inputs

A42W64AT4 shall provide two RCA type receptacles for the stereo audio signal associated with Component2 input.

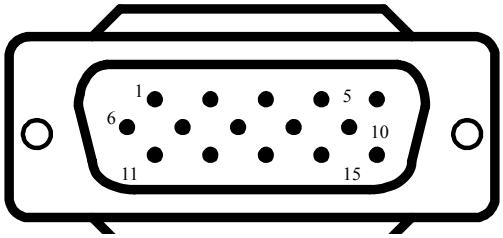
1-3-1-6 PC Input

A42W64AT4 accommodates a VGA type computer connection as specified below.

①. Video Input connector

A42W64AT4 shall provide a 15-pin D-Sub connector on its back panel for connection to a VGA type video source. The VGA signal input on the display shall be capable of receiving RGB analog video, H and V syncs, and DDC. The table below specifies pin-outs of this connector.

Analog Connector Pin-outs		
PIN	MNEMONIC	**SIGNAL**
1	RV	Red Video
2	GV	Green Video
3	BV	Blue Video
4	NC	None
5	GND	Ground (DDC Return)
6	RG	Red GND
7	GG	Green GND
8	BG	Blue GND
9	+5 V	+5 V (from the PC)
10	SG	Sync Ground
11	NC	None
12	SDA	DDC Data
13	HS	Horizontal Sync
14	VS	Vertical Sync
15	SCL	DDC Clock



②. Audio Inputs

A42W64AT4 shall provide a 3.5 mm jack for the stereo audio signal associated with VGA input.

③. Input Formats

A42W64AT4 shall support the following input format on its VGA input.

Mode	Resolution	Total	Horizontal		Vertical		Nominal Pixel Clock (MHz)
			Nominal Frequency (KHz)	Sync Pola-rity	Nominal Freq. (Hz)	Sync Pola-rity	
VGA	640x480@60Hz	800 x 525	31.469	N	59.940	N	25.175
SVGA	800x600@60Hz	1056 x 628	37.879	P	60.317	P	40.000
XGA	1024x768@60Hz	1344x806	48.363	N	60.004	N	65.000
WXGA	1280x1028@60Hz	1688x1066	64	N	60	P	108

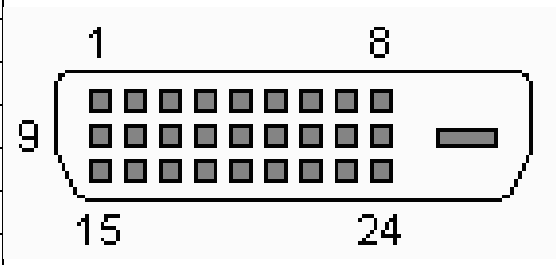
1-3-1-7 DVI

A42W64AT4 shall accommodate a DVI type digital video source as specified in this section.

①. Video Inputs

A42W64AT4 shall provide a 24 contact DVI-D receptacle on its back panel for receiving TMDS digital video. The table below specifies pin assignments for the DVI-D connector.

DVI-D Digital connector pin assignments		
PIN	**MNEMONIC**	**SIGNAL**
1	TX 2 -	TMDS Data 2 -
2	TX 2 +	TMDS Data 2 +
3	SHLD 2 / 4	TMDS Data 2 / 4 Shield
4	TX 4 -	TMDS Data 4 -
5	TX 4 +	TMDS Data 4 +
6	DDC Clk	DDC Clock
7	DDC Data	DDC Data
8	N/C	No Connect
9	TX 1 -	TMDS Data 1 -
10	TX 1 +	TMDS Data 1 +
11	SHLD 1 / 3	TMDS Data 1 / 3 Shield
12	TX 3 -	TMDS Data 3 -
13	TX 3 +	TMDS Data 3 +
14	+5V	+5V Power (from the PC)
15	GND	Ground (Return for +5V)
16	HPD	Hot Plug Detect
17	TX 0 -	TMDS Data 0 -
18	TX 0 +	TMDS Data 0 +
19	SHLD 0 / 5	TMDS Data 0 / 5 Shield
20	TX 5 -	TMDS Data 5 -
21	TX 5 +	TMDS Data 5 +
22	TX CLK SHLD	TMDS Clock Shield
23	TX CLK +	TMDS Clock +
24	TX CLK -	TMDS Clock -



②. Audio Inputs

A42W64AT4 shall provide a 3.5 mm jack for the stereo audio signal associated with DVI input.

③. HDCP support

HDCP must be supported on the DVI input. Refer to the High-bandwidth Digital Content Protection System specification version 1.1 for details.

④. Input Formats

A42W64AT4 shall support the following input format on its DVI input.

Mode	Resolution	Total	Nominal HFrequency (KHz)	Nominal Vertical Frequency (KHz)	Nominal Pixel Clock Frequency (MHz)
VGA	640x480@60Hz	800 x 525	31.469	59.940	25.175
SVGA	800x600@60Hz	1056 x 628	37.879	60.317	40.000
XGA	1024x768@60Hz	1344x806	48.363	60.004	65.000
720P	1280×720P		45.00	60	74.25
1080i	1920×1080i		33.75	60	74.25
480p	720×480p		31.54	60	27.00

1-3-2 Power Interface

1-3-2-1 Power Connector

A42W64AT4 shall support an IEC C-13/C-14 (Standard) type male power receptacle for connection to AC power source.

1-3-2-2 Power Input Range

The operating range shall be from 100 to 240 VAC sinusoidal. Input power frequency range shall be from 50 to 60 Hz over the specified input voltage range.

1-3-2-3 Power Consumption

①. Operating Power

Power consumption for the display over the specified voltage and frequency ranges shall be less than 350 W for the assemblies with speakers.

②. Standby Power

A42W64AT4 power also below than one watt in the standby mode.

1-3-3 Service Interface

A42W64AT4 shall provide a 9-pin D-sub connector on its back panel for firmware upgrading purpose. This interface shall conform to RS-232 standard with the following pin-outs.

Pin	Function
1	NC
2	TXD transmitted data
3	RXD received data
4	Shorted with pin 6
5	FG frame ground
6	Shorted with pin 4
7	Shorted with pin 8
8	Shorted with pin 7
9	NC

The method of firmware upgrading please see **“Flash update process”** chapter.

1-4 User interface

1-4-1 Power Indicator

A42W64AT4 shall make use of an LED type indicator located on the front of the display. The LED color shall indicate the power states as given in the following table.

LED colors

Mode	H-Sync	V-Sync	Video	Pw-cons.	Indicator
Power-On	On	On	Active	＜350W	Blue LED
Standby	Off	Off	Off	＜1W	Red LED

1-4-2 Remote Control Receiver

A42W64AT4 shall provide an infra-red (IR) optical detector on its front panel for use as the receiver for remote controller signal. The IR communication protocol shall conform to RC-5 standard. The minimum IR reception angles shall be +/- 30 degrees horizontally and vertically. The required operating distance of the remote control shall be 7 m.

1-4-3 On-Screen Display

A42W64AT4 shall provide an On Screen Display (OSD) system for customer setup. The following table gives the structure of the OSD menus.

Main menu	Sub menu	Function	Default	Reset
SETUP	Tuning Band	To select between Air and Cable System	Air	—
	DTV Signal	To display the signal strength in order to aid the antenna adjustment	—	—
	Auto Ch Search	To automatic scan and store all TV channels	—	—
	Manual Ch Set	To enable or disable channels	—	—
	Channel Label	To rename a channel	—	—
	Manu Language	To select the language for OSD among English, Spanish, French, and Portuguese	English	—
VIDEO	CONTRAST	To adjust the contrast value between 0~100	50	Yes
	BRIGHTNESS	To adjust the brightness value between 0~100	50	Yes
	SHARPNESS	To adjust the sharpness value between 0~100	50	Yes
	COLOR	To adjust the color value between 0~100	50	Yes
	TINT	To adjust the tint value between 0~100	50	Yes
	Aspect Ratio	To select aspect ratio among Normal, Zoom, Wide, and Cinema	Normal	Yes
	Settings	To restore all video settings to factory default	—	—
AUDIO	Audio Language	To select audio language among English, Spanish, French, and Portuguese	English	Yes
	BASS	Sets the bass value between 0~100	31	Yes
	TREBLE	Sets the treble value between 0~100	31	Yes
	BALANCE	Sets the left/right balance value between 0~100	31	Yes
	Restore Default	To restore all audio settings to factory default	—	—
FEATURE	Time Set	To set current time	—	—
	Sleep Timer	To set the timer period to turn off the TV. Selectable values are OFF,30,60 and 90 minutes	OFF	—
	Password Set	To set or change Parental Control password	TBD	—
	Parental Control	To select V CHIP settings	Un-locked	—
	White Screen	To make a White screen by TV ifself.	—	—

1-5 External Mounting Requirements

A42W64AT4 shall be designed so that the display enclosure can be easily removed from the base for external mounting applications. When the base is removed, there shall be no additional non-removable parts that are visible from the front of the display

1-6 Environmental Requirements

1-6-1 Temperature Ranges

Operating Temperature (Independent of altitude) ..... 0°C to 40°C
Non-Operating Temperature (Independent of altitude) .... -10°C to 70°C

1-6-2 Humidity

Operating (non-condensing) ....20% to 85%
Non-Operating (38.7°C maximum wet bulb temperature..... ....5% to 85%

1-6-3 Altitude

Operating .... (0 to 2,000 m)
Non-Operating..... .... (0 to 3,000 m)

1-6-4 Vibration and Shock

All testing shall be done in each of three mutually perpendicular axes, referenced to the position of the system as it is in front of the user (i.e., front-to-back, side-to-side, and top-to-bottom).

2、Precautions and Notices：

2-1 Precaution of assembly

（1）Please do not press or scratch PDP panel surface with anything hard.
（2）Please wipe out PDP panel surface with absorbent cotton or soft cloth in case of it being soiled
（3）Please wipe out drops of adhesive like saliva and water in PDP panel surface immediately. They might damage to cause panel surface variation and color change
（4）Do not apply any strong mechanical shock to the PDP panel

2-2 Precaution of Operation：

（1）Please be sure to unplug the power cord before remove the back-cover. (make sure the power is turn-off)
（2）Please do not change variable resistance settings in PDP MODULE; They are adjusted to the most suitable value. If they are changed, it might happen LUMINANCE does not satisfy.
（3）Please consider that PDP MODULE takes longer time to become stable of radiation characteristic in low temperature than in room temperature.
（4）Please pay attention to displaying the same pattern for very long-time. Image might stick on PDP.

3、Operation

3-1 Operation of Remote Control Transmitter

A42W64AT4 shall provide an IR remote controller as accessory.

"Wide Mode"
Normal, Zoom ,Wide, Cinema display select

"EPG"
Display the state, source

"TV"
TV source select, into TV state

"SLEEP"
Select timer into power down state. off→30→60→90→off

"CC"
To select close caption options(CC1,CC2……)

"ENTER"
To enter sub Menu or sub item .

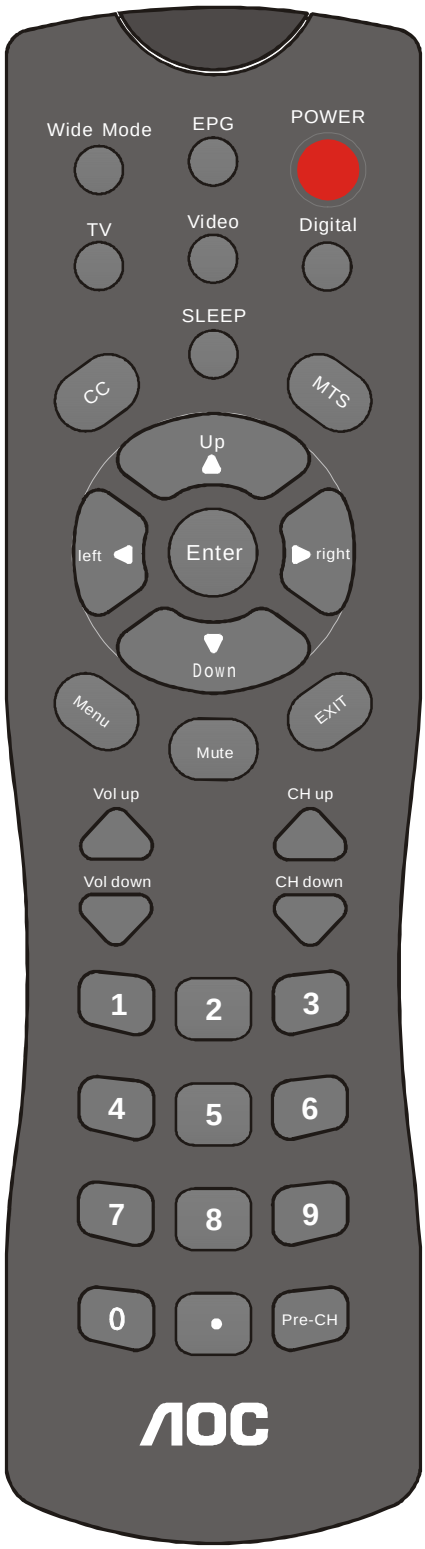
"MENU"
To enter Menu mode .

"MUTE"
Mute the sound

"Vol up / Vol down"
Press Vol up/ Vol down key to adjust volume .

"0~9 number"
To enter TV channel number

" ● "
To enter sub channel number for digital channels .



"POWER"
The TV Set turn on /turn off kev

"Video"
AV1 CVBS Rear /AV1 S-Video Rear/ AV2 CVBS Side/ AV2 S-Video Side / AV3 component 1/ AV4 component 2

"Digital"
VGA/DVI source input

"MTS "
To select audio program options

"Up▲/Down▼"
Move the cursor up and down on the Menu

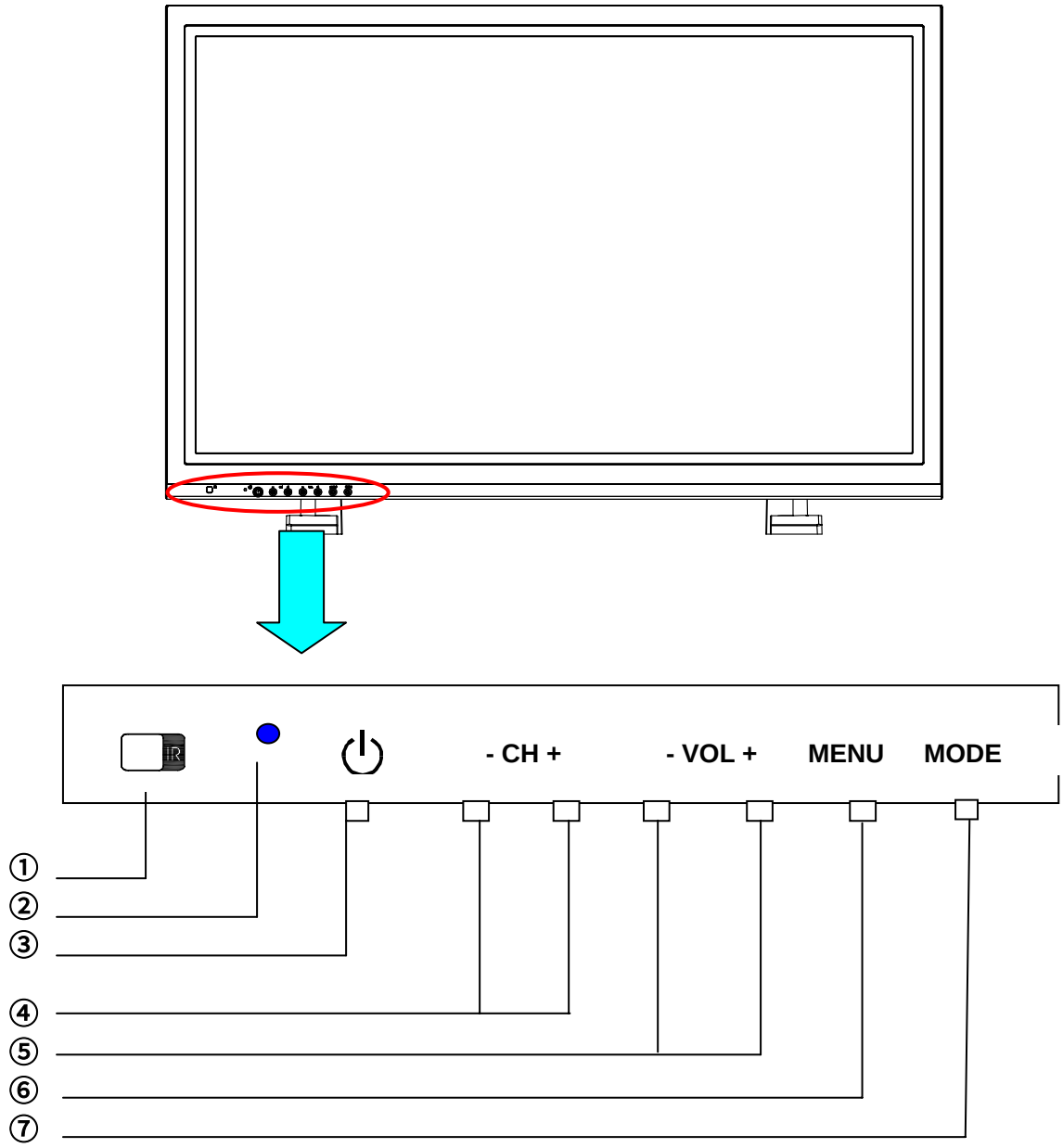
"left ◄ / right ►"
Use left ◄/ right ► to select or adjust an item.

"EXIT"
To exit Menu or other OSD .

"CH up / CH down"
Press to select the next lower or higher Program number.

"Pre-CH"
TV channel return, see last TV channel .

3-2 Front panel controls

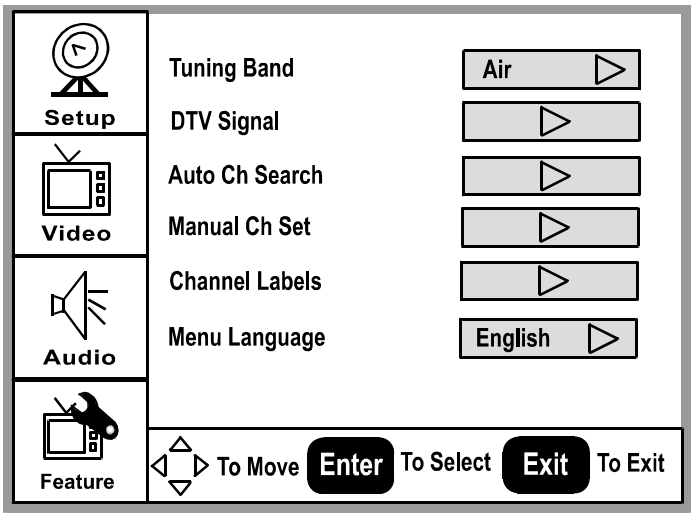


①	IR: Remote Control Sensor.
②	LED: Power Indicator.
③	Power switch: Press to power on or power off the TV set..
④ -CH+	Down: Press to select the next lower Programme number or move Down in Menu operation. Up: Press to select the next higher Programme number or move up in Menu operation.
⑤ -VOL+	Left: Press to decrease the sound volume level or move Left in Menu operation. Right: Press to increase the sound volume level or move Right in Menu operation.
⑥ MENU	Menu: Press to enter Menu or exit Menu.
⑦ MODE	Mode: Press to select input signal modes or use as Enter in Menu operation.

3-3 OSD MENU Description

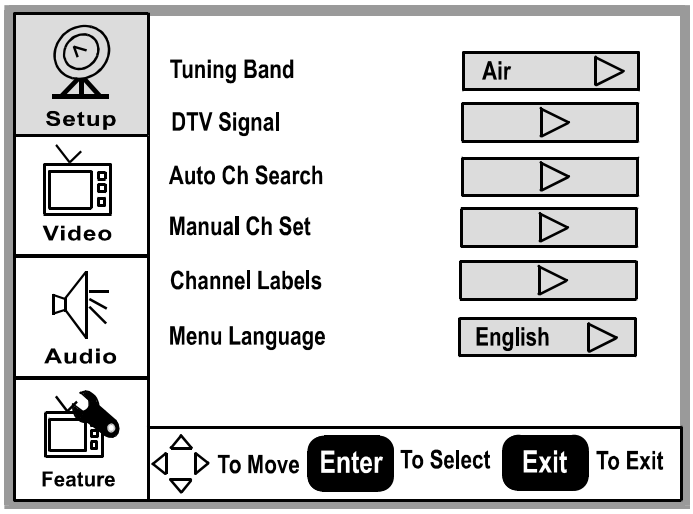
3-3-1 Main MENU

1. Press “MENU” key on remote control or front panel controls to bring up Main Menu.
2. Press “▲” or “▼” to move the cursor up and down the sub menu list.
3. Press “◀” or “” to select sub menu item.
4. Press "Enter" to enter sub-item then use “◀” or “▶” to adjust.

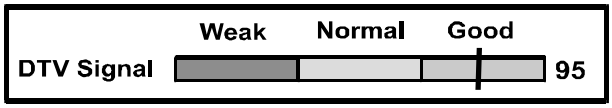


3-3-2 SETUP MENU

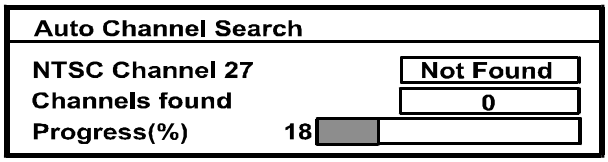
1. Tuning Band: Select TV signal source between Air and Cable. Select Cable if you are connecting to a cable box and select Air if you are directly connecting to the antenna.
2. DTV Signal: Display signal strength to aid antenna adjustment.
3. Auto Ch Search: Automatically scan and store all TV channels.
4. Manual Ch Set: Enter channel setup table.
5. Channel Labels: Display and edit channel names.
6. Menu Language: Select language for menu (English→Español→Fançais→Portuguese).



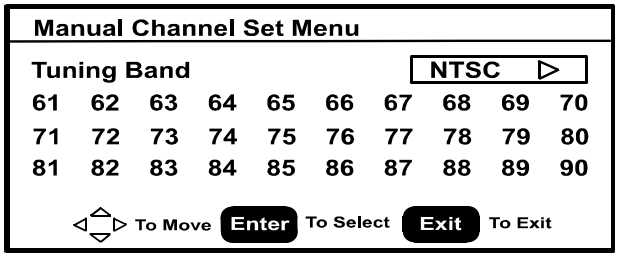
- DTV signal menu indicates signal strength in real-time.



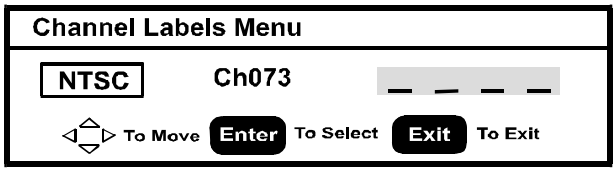
- Auto channel scan menu displays channel number being scanned.



- Manual Channel Set Menu
  Displays all the channel numbers that are found.
  Tune either to ATSC or NTSC channels.
  Add or delete Channel number.

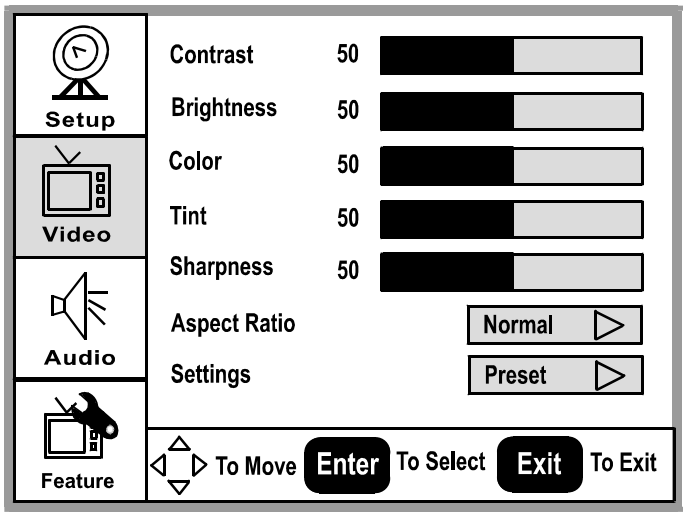

Manual Channel Set Menu
Tuning Band
NTSC
61 62 63 64 65 66 67 68 69 70
71 72 73 74 75 76 77 78 79 80
81 82 83 84 85 86 87 88 89 90
To Move
Enter
To Select
Exit
To Exit

- Channel Labels Menu allows user labeling.



3-3-3 Video MENU

1. Press “▲” or “▼” to move the cursor up or down the sub-item list.
2. Press "Enter" to enter the highlighted sub-item menu.
3. Press “◀” or “ ▶” to adjust the value of the sub-item.
4. Press "Enter" again to exit the sub-item.



Contrast: Contrast adjustment, 0~100.

Brightness: Brightness adjustment, 0~100.

Color: Color chroma adjustment, 0~100.

Tint: Tint adjustment, 0~100.

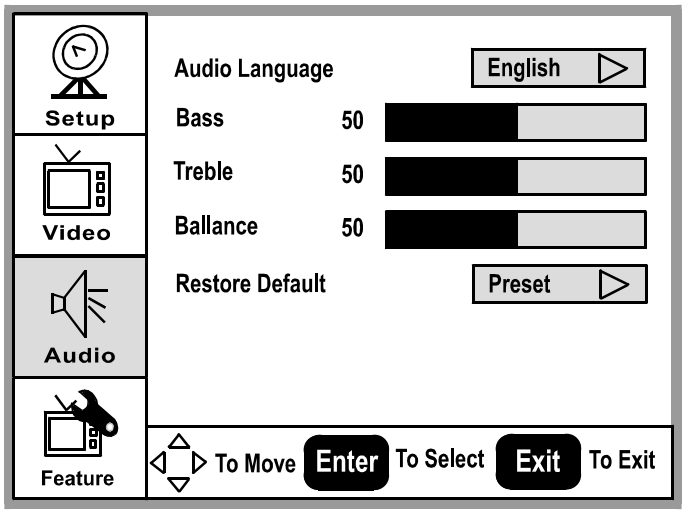
Aspect Ratio: Aspect Ratio selection.

Normal➙Zoom➙Wide➙ Cinema.

Settings: Restore default setting.

3-3-4 Audio MENU

1. Press “▲” or “▼” to move the cursor up or down the sub-item list.
2. Press "Enter" to enter the highlighted sub-item menu.
3. Press “◀” or “▶” to adjust the value of the sub-item.
4. Press "Enter" again to exit the sub-item.



Audio Language:

English➙Español➙Français➙Portuguese.

Bass: Bass adjustment, 0 ~ 100.

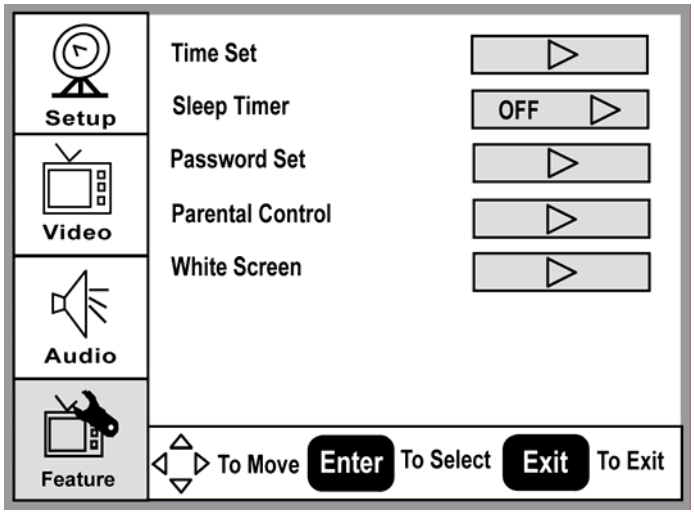
Treble: Treble adjustment, 0 ~ 100.

Balance: Balance adjustment, 0 ~ 100.

Restore Default: Restore Audio Language, Treble, Base, and Balance setting to default.

3-3-5 Feature MENU

1. Press “▲” or “▼” to move the cursor up or down the sub-item list.
2. Press "Enter" to enter the highlighted sub-item menu.
3. Press “◀” or “▶” to adjust the value of the sub-item.
4. Press "Enter" again to exit the sub-item.



Time Set: Select minutes into standby Off → 30 → 60 → 90.

Password Set: Enter and change Parental Control Password.

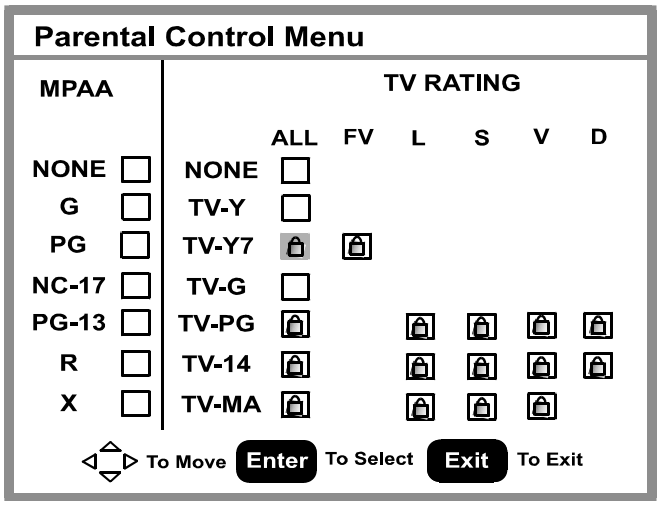
Parental Control: Setup TV and Movie rating controls.

White Screen: Select White Screen, and press MODE front panel button (Enter on the Remote control).The TV immediately displays the white screen.

Parental Control Menu: Controls viewing of rated TV and Movie programs.

Default password is: 0000.

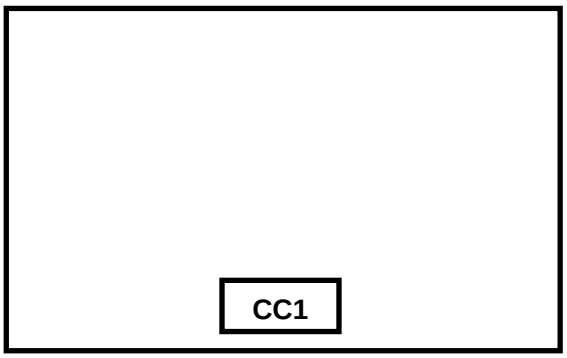
Important : If you have forgotten your Password. Use the code [0711] to enter into the Password Set menu item to change your password. You can also use the code [0711] to change your Parental Controls settings.



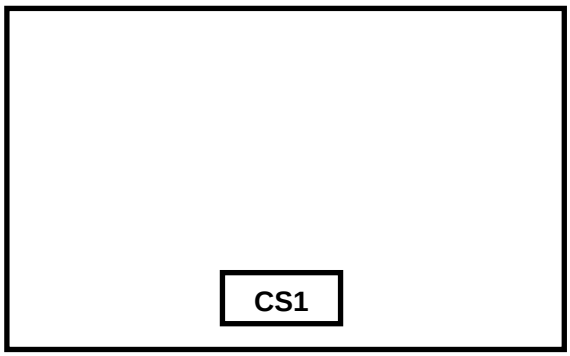
3-3-6 Closed Captions

1. Press “CC” key on remote control to select closed captions mode.
   NTSC TV: Off CC1 CC2 . …
   ATSC TV: Off CS1 CS2 . …
2. Select desired closed caption mode.

3.Closed captioning for analog NTSC channels is transmitted as CC1/CC2/CC3/ CC4. Closed captioning for digital channels is transmitted as CS1/CS2/CS3/CS4/ CS5/CS6 or occasionally CC1/CC2/CC3/CC4. You need to select the option you want for analog channels and digital channels separately.



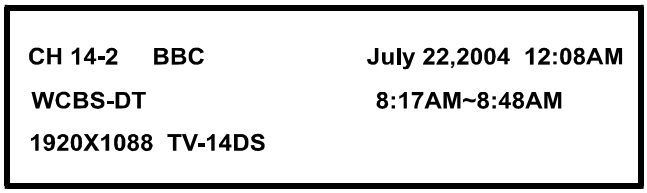
□ NTSC TV



□ ATSC TV

3-3-7 EPG

Press the “EPG” key on the remote control to display the Electronic Program Guide (EPG). A message window will be displayed on screen.



□ EPG Message Window

3-3-8 TV channel arrangement

Each digital channel may comprise of several sub-channels.
To select a digital channel using the remote control:
1. Enter main channel number.
2. Press the “•” key.
3. Enter the sub-channel number.

4、Trouble shooting chart

If replace “IMAGE BOARD”, Please re-do “DDC writing” program & “WHITE-BALANCE” & Flash Update.

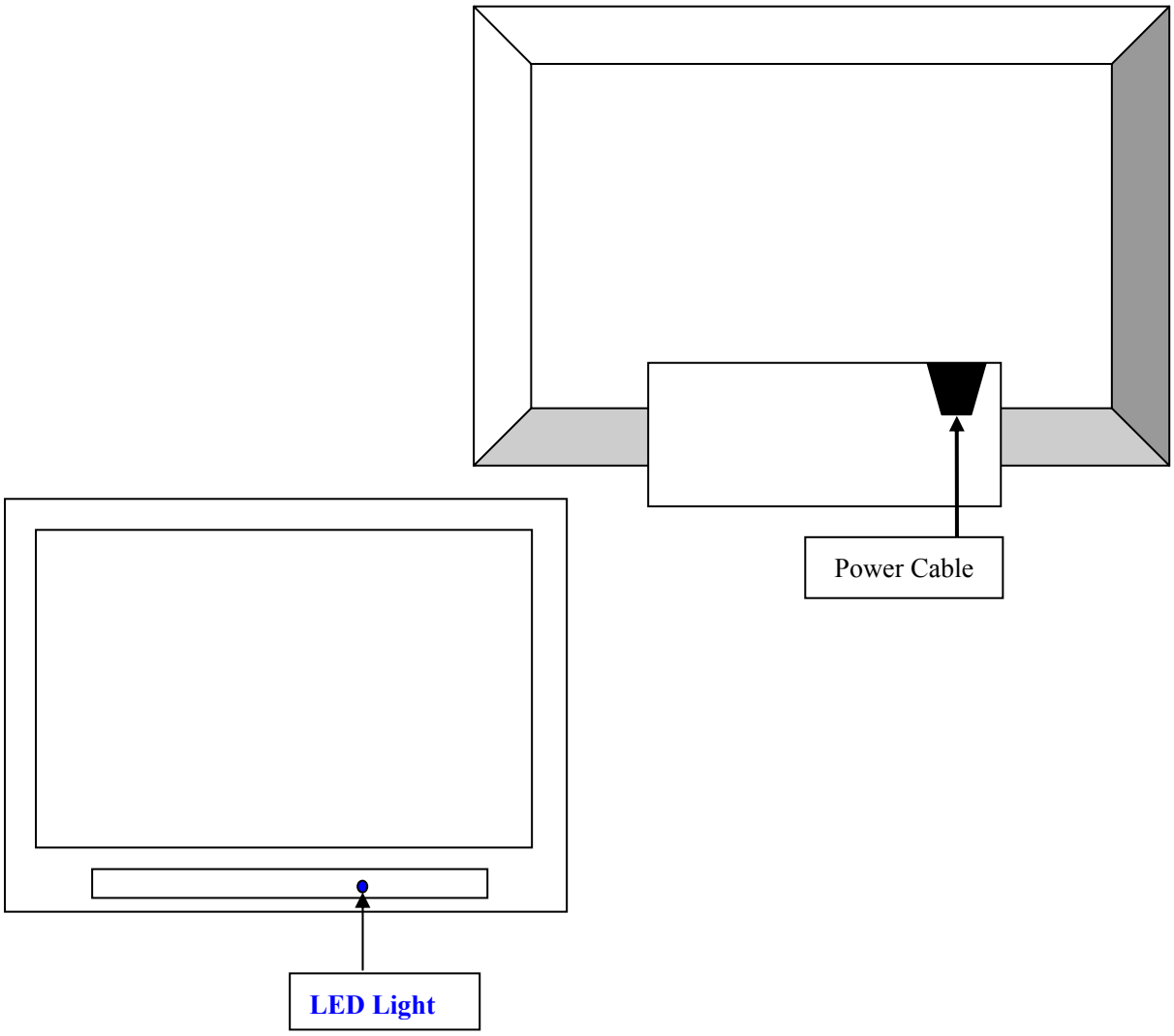
If replace PANEL module, Please re-do “white-balance adjust”

4-1 PANEL Trouble shooting

Please reference the “PANEL Service Manual”.

4-2 Turn PDP on and Check:

Plug power cord into pdp set, and the color of LED is red;



If PDP under the normal working, display of LED is blue. Then, the screen show is nor dark. If the color of LED is red under standby state, you should press the “power” bottom of remote control or you should press the front standby key. Then, turn PDP TV on.

If it is nothing about OSD or display on screen, service PDP.
The procedure and maintain the step meet as follows:

4-2-2 Solution process of whole PDP:

Screen is nothing under power on

Check AC input of PDC

Check PowerSTB5V（U516 3PIN）
Voltage: 5V

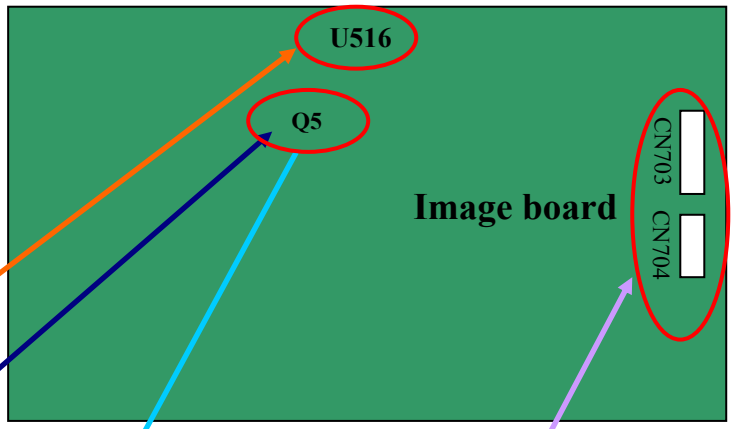
Check the REL-SW state of power IO interface，
High Voltage：Turn on
Low Voltage：Standby
Test Point： C pole of Q5
High Voltage：5V（4.2---5.3V）
Low Voltage：0V

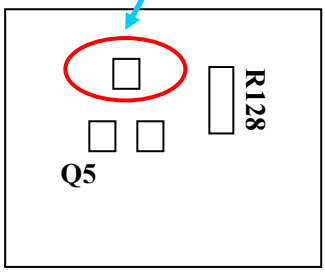
If REL-SW is ok，check other power.

Check device circuit and logic circuit, Vs, Vset, Vsc, Ve etc.
Arrow shows test point.

If there was anything unmoral, test voltage and repair it.

Process of repair as follow





Check the voltage of CN703：
PIN5 --→ 12 V
PIN8 --→ 3.3 V
PIN9 --→ 3.3 V
PIN11 --→ 6 V (Samsung PANEL)

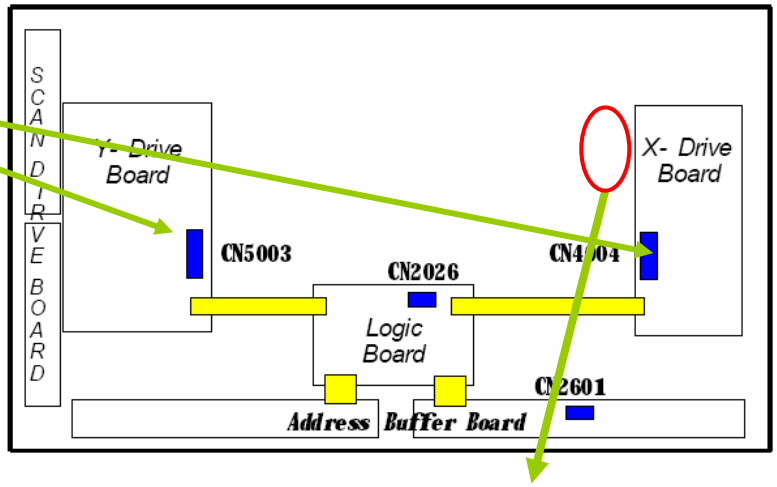
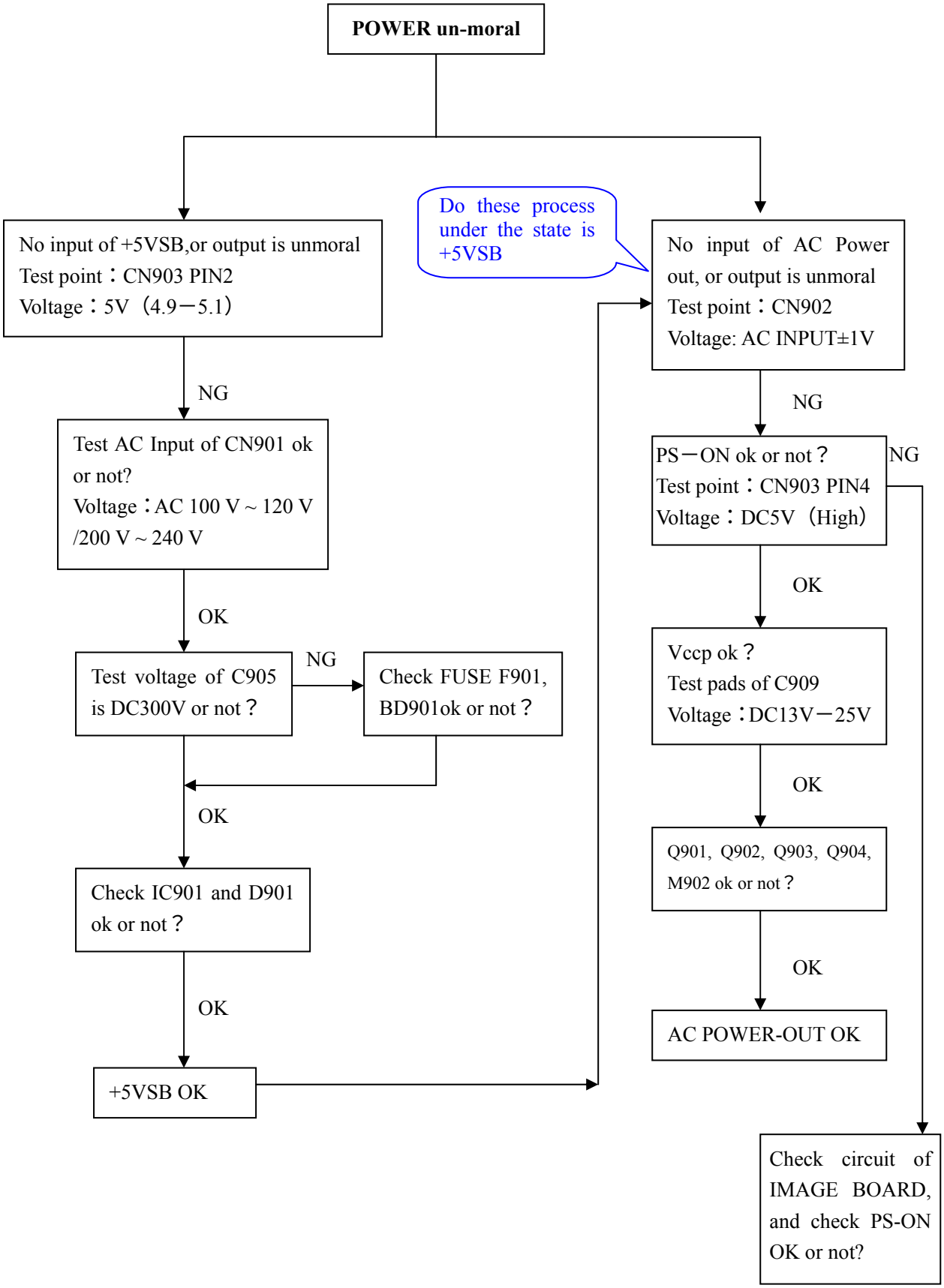


Fig1: Voltage sheet

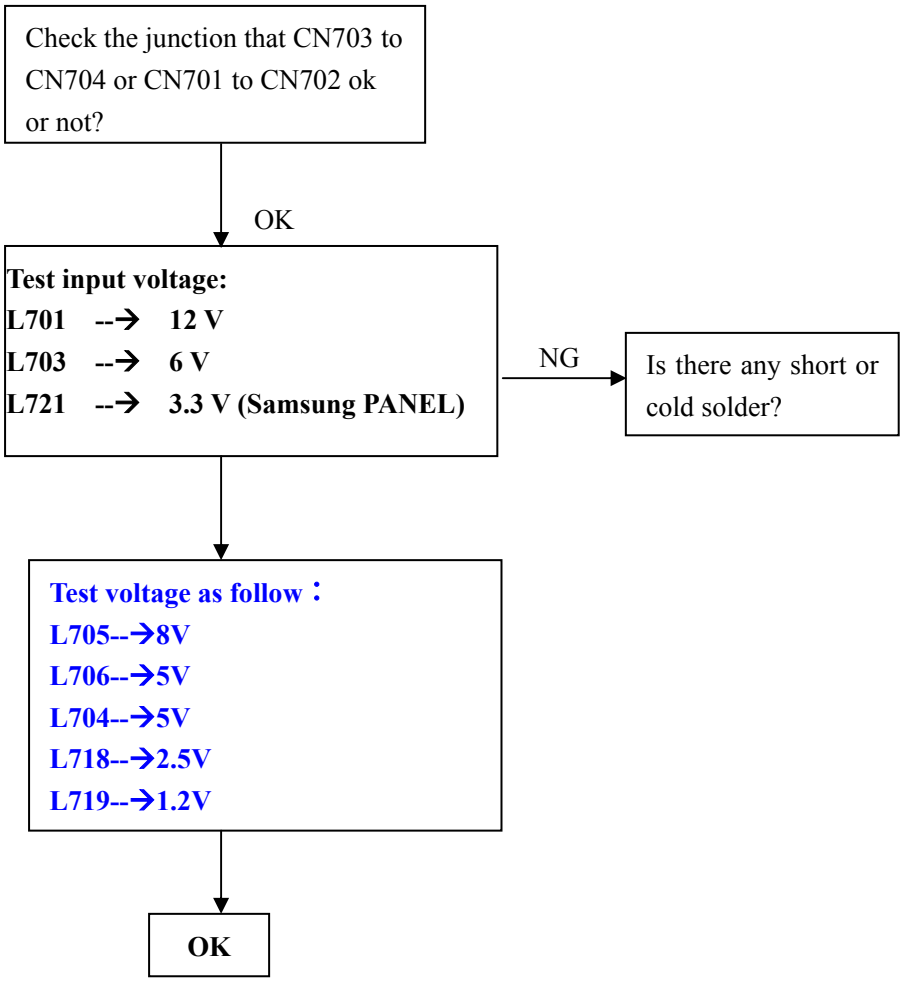
Name	Voltage	Reference
VS	209V	Voltage for driving sustain
VA	70V	Voltage for driving address
VE	82V	Voltage for driving X-bias
VSET	198V	Voltage for driving reset
Vscan	-198V	Voltage for driving scan
Vg	15V	Voltage for driving FET
D3V3	3.5V	Voltage for driving logic

4-2-3 STB POWER Solution process

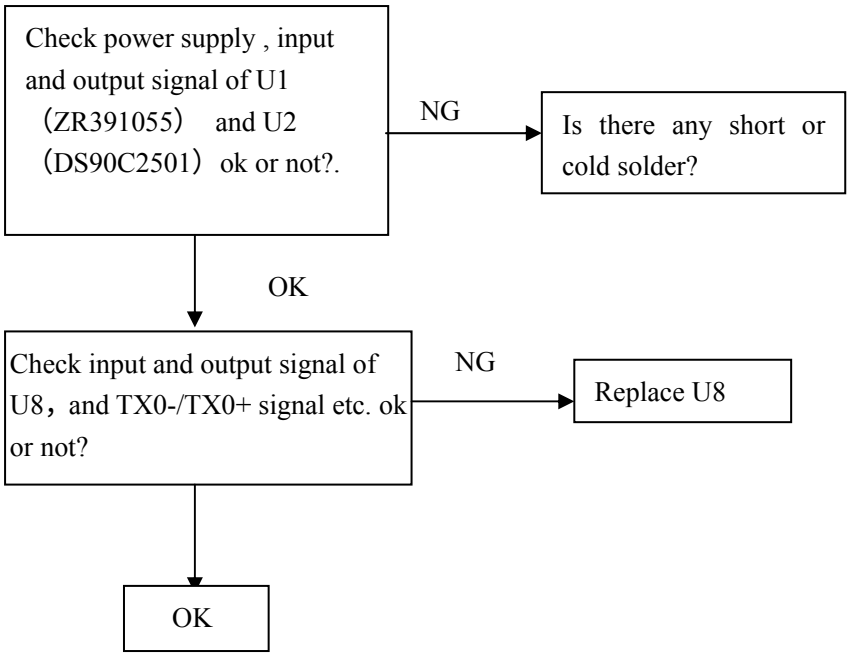


Note：Must distinguish connect Grand point of Power primary and secondary level.

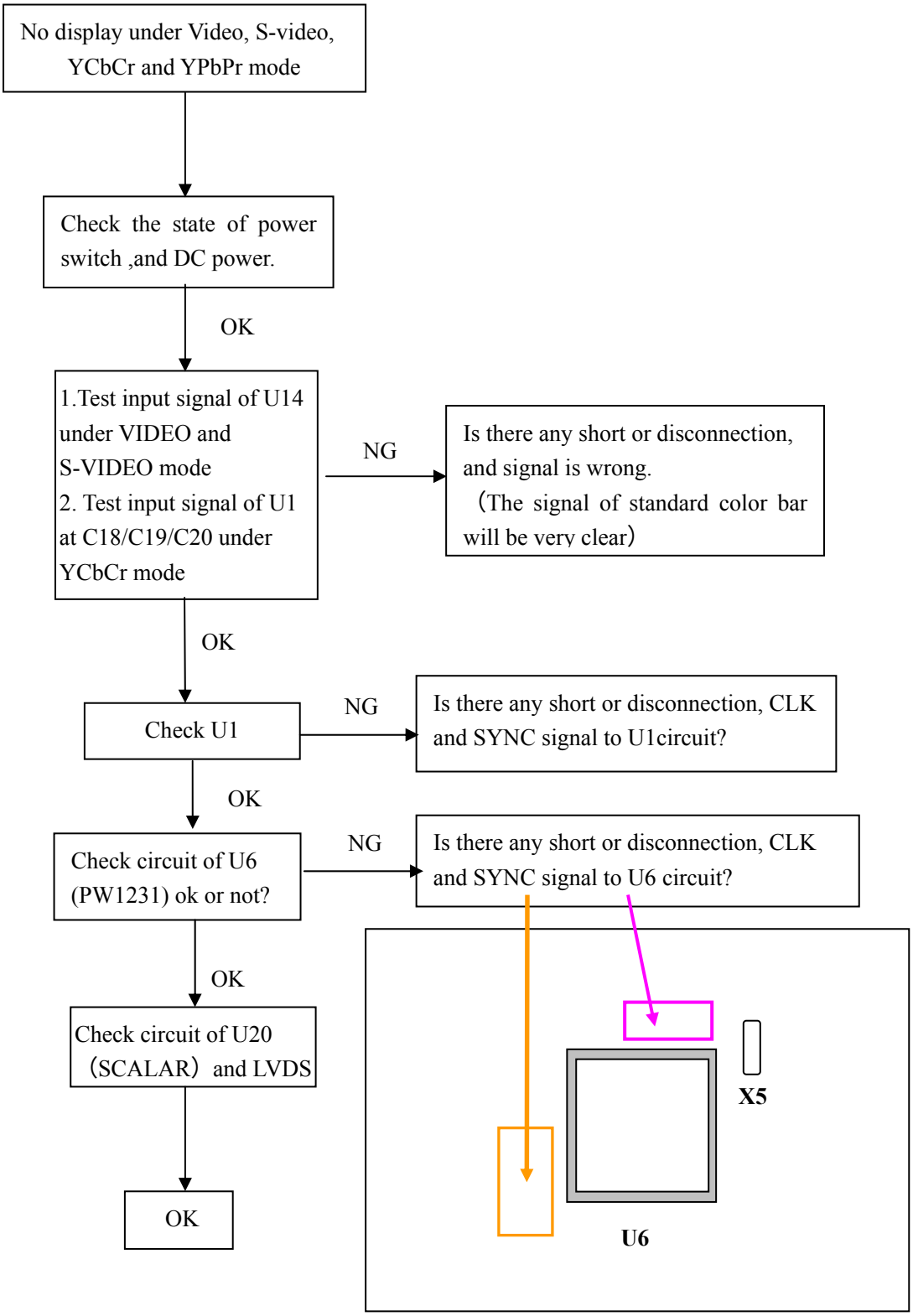
4-2-4 Solution processes for DC Power



4-2-5 Solution processes for SCALER


Check power supply , input and output signal of U1 （ZR391055） and U2 （DS90C2501） ok or not?.
NG
Is there any short or cold solder?
OK
Check input and output signal of U8，and TX0-/TX0+ signal etc. ok or not?
NG
Replace U8
OK

4-2-6 Solution processes VIDEO


No display under Video, S-video, YCbCr and YPbPr mode
Check the state of power switch ,and DC power.
OK
1.Test input signal of U14 under VIDEO and S-VIDEO mode
2. Test input signal of U1 at C18/C19/C20 under YCbCr mode
NG
Is there any short or disconnection, and signal is wrong.
（The signal of standard color bar will be very clear）
OK
Check U1
NG
Is there any short or disconnection, CLK and SYNC signal to U1circuit?
OK
Check circuit of U6 (PW1231) ok or not?
NG
Is there any short or disconnection, CLK and SYNC signal to U6 circuit?
OK
Check circuit of U20 （SCALAR） and LVDS
OK
X5
U6

5、White-Balance Adjustment

5-1 Equipments list

Chroma7100	1set
VG828 video signal generator	1set
Chroma-2326	1set

5-2 Preparation and Adjustment process

1、Preparation:

- Connect rear Video port of PDP with AV port of VG-828.
- Connect component port of PDP with YPbPr port of VG-828
- Connect VGA port of PDP with corresponding port of Chrom2326
- Turn power of PDP and test instrument on.
- Before open lens, Press O-CAL of Chrom-7100 and revise lens.

2、Adjustment process

AV Adjustment

1). Change to Video mode, you can press “SOURCE” of remote. Press “Vol - ”, adjust volume until Min. Then press number key “6543”and enter factory Menu.

2). Press “SOURCE” and change to Video Rear mode

3). When setting of VG-828 is TIM946/PAT922, 32 Gray steps. Then, see the color of picture is deflection or not. And the Gray steps distinguish 28 steps from 32steps or not.

①. If dark of Gray is deflection, press “CH+/-”and adjust:

1.White.BRoCVBS (vMin=0,vMax=100,vDef=50) →50,
2.White.BBoCVBS (vMin=0,vMax=100,vDef=50) →50,
3.White.BGoCVBS (vMin=0,vMax=100,vDef=50) →50,

②. If sharpness of Gray is deflection, press “CH+/-”and adjust:

4.White.BRgCVBS (vMin=0,vMax=100,vDef=50) →50,
5.White.BBgCVBS (vMin=0,vMax=100,vDef=50) →50,

4). When the Gray is ok, change input signal to white picture at P936, Use colored analysis instrument Chroma7100 measure colors temperature value of picture at present (whether Chroma7100 is it given to picture center to pop one's head), On pressing the remote controller such as the specification of going beyond "program + /- "key choose following the projects adjust：

4.White.BRgCVBS (vMin=0,vMax=100,vDef=50) →50,
5.White.BBgCVBS (vMin=0,vMax=100,vDef=50) →50,

5). When adjustment about white is ok, changes signal to P822 that Gray steps picture. The Gray picture has no deflection color, and the Gray steps distinguish 28 steps from 32steps

Note: The white balance is adjusted in the course, will influence each other to adjust in the adjustment of gray steps and white picture, and need to change repeatedly.

Please notice that can't enter the mode of the factory in every station homework after adjusting and finishing, so as not to miss movements and revise the white balance data again.

VGA Adjustment

Setting of Chroma2326 as follows:

Gray picture: TIM4/PAT48

White picture: TIM4/PAT105

Change to VGA mode, press "CH+/-"and adjust following items. Method same as AV mode:

6. White.BRoVga (vMin=0,vMax=100,vDef=50) →50,
7. White.BBoVga (vMin=0,vMax=100,vDef=50) →50,
8. White.BGoVga (vMin=0,vMax=100,vDef=50) →50,
9. White.BRgVga (vMin=0,vMax=100,vDef=50) →50,
10. White.BBgVga (vMin=0,vMax=100,vDef=50) →50,

Note: Press "Source" and change mode that Video Rear to VGA, then adjustment items of white balance same as Video Rear First, press "CH+/-" and adjust under the VGA mode. (White.BBgCVBS(vMin=0,vMax=100,vDef=50)→50 CVBS change to VGA)

COMPONENT Adjustment:

1). VG828 setting as follow：

Gray picture：TIM954/PAT922

White picture：TIM954/PAT936

2). Change to COMPONENT1 mode，press "CH+/-"and adjust following items. Method same as AV mode：

1. White.BRoVga (vMin=0,vMax=100,vDef=50) →50,
2. White.BBoVga (vMin=0,vMax=100,vDef=50) →50,
3. White.BGoVga (vMin=0,vMax=100,vDef=50) →50,
4. White.BRgVga (vMin=0,vMax=100,vDef=50) →50,
5. White.BBgVga (vMin=0,vMax=100,vDef=50) →50,

Adjustment stand of white Balance： x=299±15，y=315±15

6、DDC program and test

6-1 Equipments list and prepare

DDC tester	1PCS
PC	1SET
D-SUB cable	1PCS
DVI cable	1PCS
Barcode Reader	1SET

Prepare before test:

1. Turn on the power of your PC and programmer, then make good connection of them.
2. Connect the D-SUB wire and DVI wire to the DDC program equipment and the PDP monitor.

6-2 Program and test process

1. Choose different DDC menu according to different customer , do use PAGE DOWN/PAGE UP to go to the submenu and parent menu until find the right model. Press enter to access the program interface. There will be shown RGB on the screen. Then switch to RGB program on the DDC connector。 Press any key to access RGB program interface ,then there will be “input serial no.:” prompt on the screen.

2. Use Bar Readers to read the serial no to the program，then make sure the serial no you have read is the same as on the barcode. Then set the PDP to blue screen mode, press enter to start.

3. Watch the information of the program, it means programmed OK when the following interface come out. please CHECK Manufacturer Name、Vendor Assigned Code、Model Name、Serial Number：****[??????????****](same as Barcode)、Week of Manufacture：**、Year of Manufacture：****、Checksum：**（same as the last byte of data table, reference to the note of RGB programming picture）and so on.

4. Press Enter to access RGB DDC test interface，follow the DDC test picture，CHECK Manufacturer Name、Vendor Assigned Code、Model Name、Serial Number：****[??????????****](same as Barcode)、Week of Manufacture：**、Year of Manufacture ****、Video Input：Analog、Checksum：**（same as the last byte of data table, reference to the note of RGB programming picture）and so on.

5. Press any key to access DVI program interface, there will be “DVI” shown on the screen. Switch the of switch on the DDC connector, press any key to access DVI program interface, there will be “input serial no.:” promote.

6. Use Bar Readers to read the serial no to the program，then make sure the serial no you have read is the same as on the barcode. Then set the PDP to blue screen mode, press enter to start.

7. Watch the information of the program, it means programmed OK when the following interface come out. please CHECK Manufacturer Name、Vendor Assigned Code、Model Name、Serial Number：****[??????????****](same as Barcode)、Week of Manufacture：**、Year of Manufacture：****、Checksum：**（same as the last byte of data table, reference to the note of DVI programming picture）and so on.

8. Press Enter to access DVI DDC test interface，follow the DDC test picture，CHECK Manufacturer Name、Vendor Assigned Code、Model Name、Serial Number：****[??????????****](same as Barcode)、Week of Manufacture：**、Year of Manufacture ****、Video Input：Analog、Checksum：**（same as the last byte of data table, reference to the note of DVI programming picture）and so on。If the recording is failure, check the connection of equipment and record again from the step4.If all of these work does not take work ,please ask IE department for help.

9. Notice :the “?” and “*” symbol will be changed according to the year of manufacture ,and so on.

7、Flash Update

7-1 The list of Instrument

1、Prepare 1 piece of RS232 cable（The Pin connection see the Figure-1，If difference, please re-connect the cable）and 1 set of PC.

2、 Connect the RS232 cable with PC and PDP(See the Figure-2).

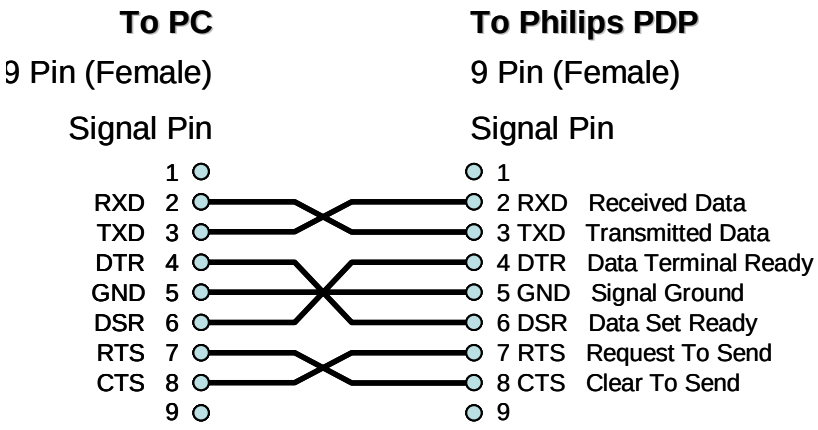


Figure-1

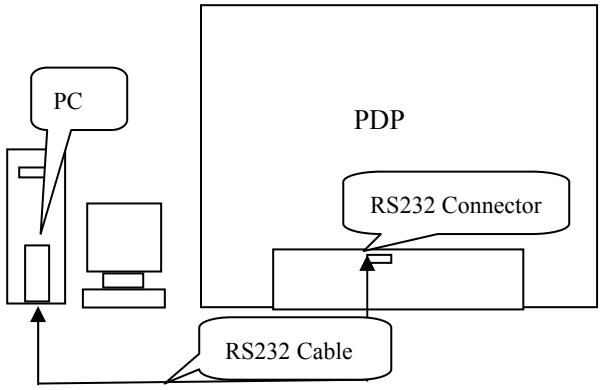


Figure-2

7-2 The operation explaining Flash Update

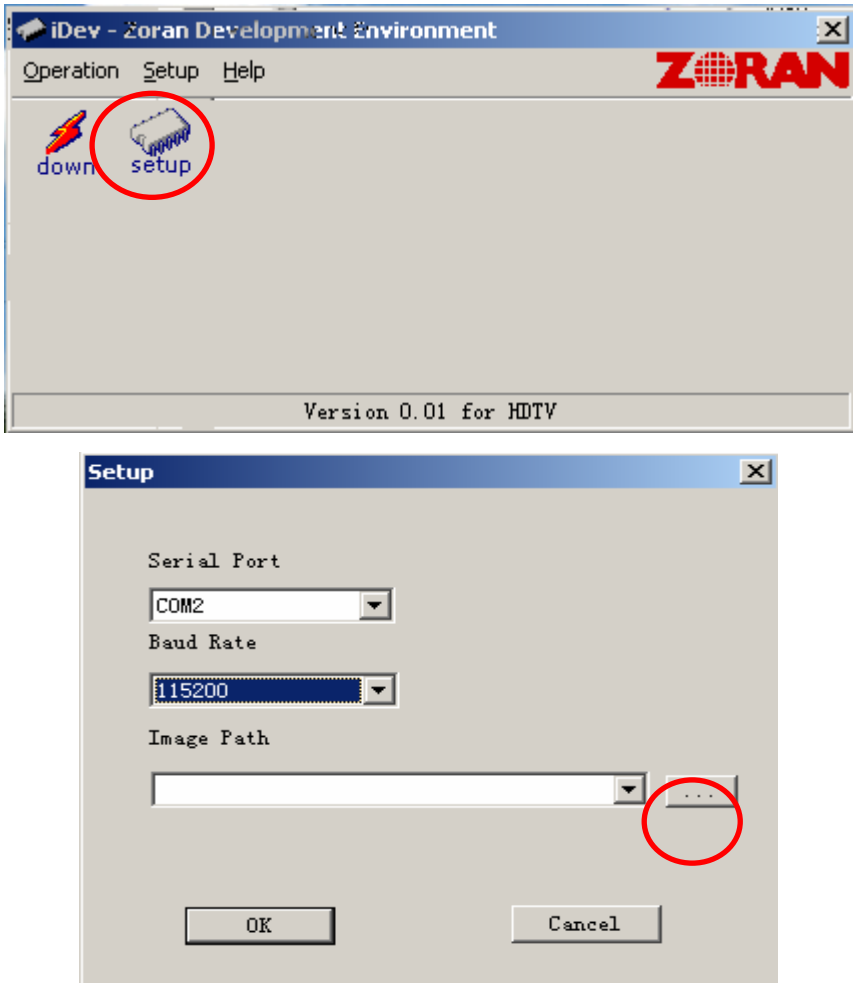
Note: Operation Under the situation of PDP working normally.

The iDev is a Windows utility that installs hex files into the FLASH ROM of the target Image Processor system. iDev is a Windows-based application.

Downloading is done through an RS-232 connection, which is bidirectional and serial.

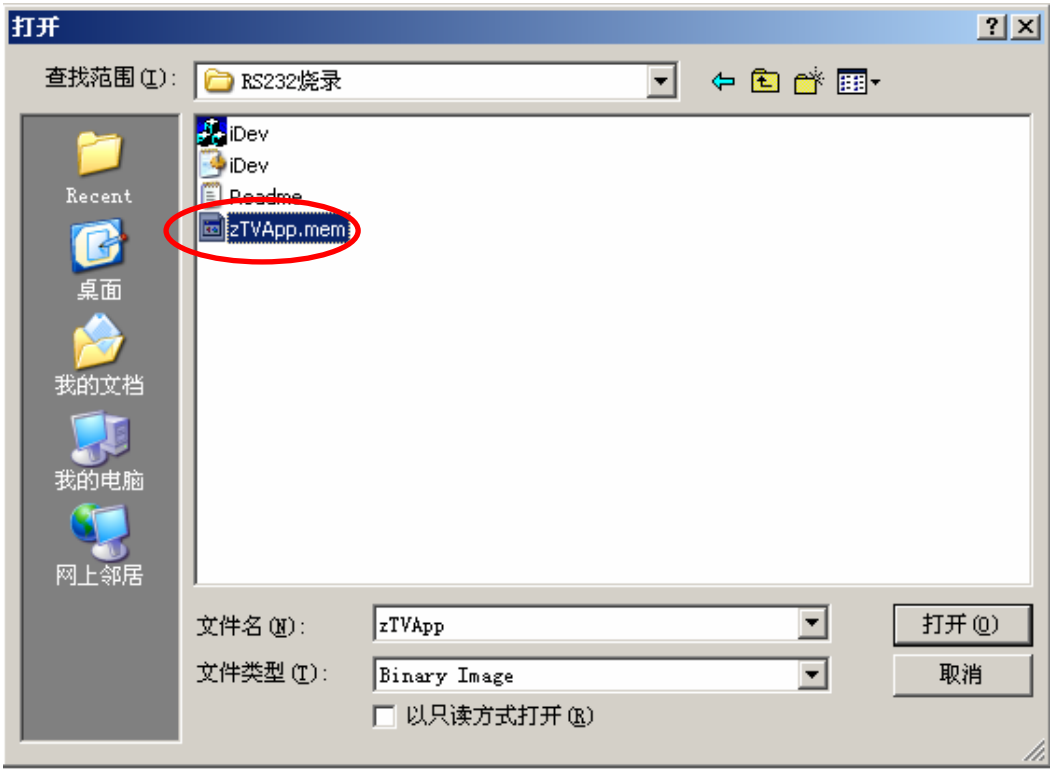
Step 1: Open the file iDev (You should

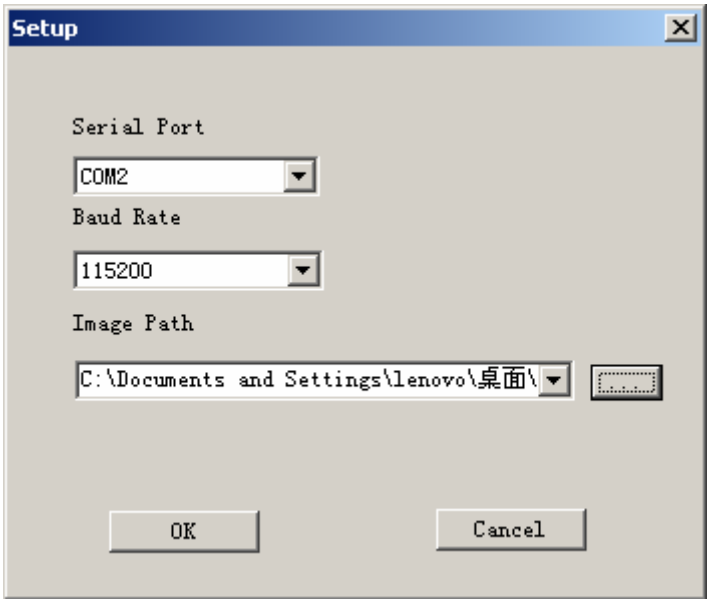
Step 2: Choose the director of the file to flash



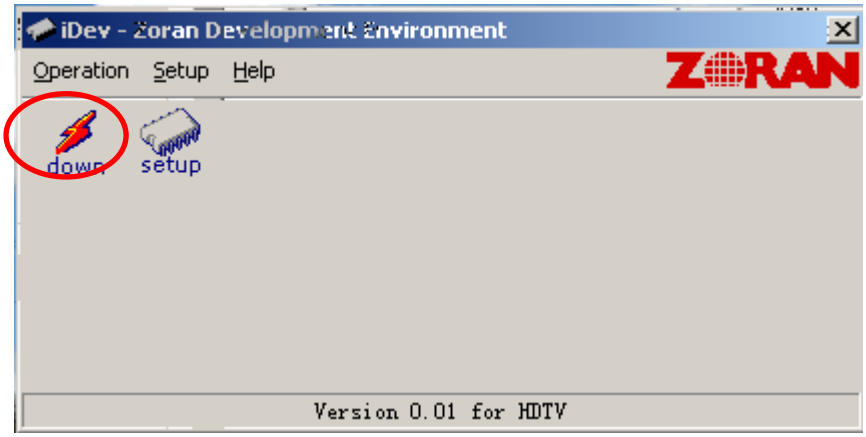
Note: Connect the computer's serial port (usually COM1) to the serial port of the ZORAN evaluation board using a null modem cable, and select speed.

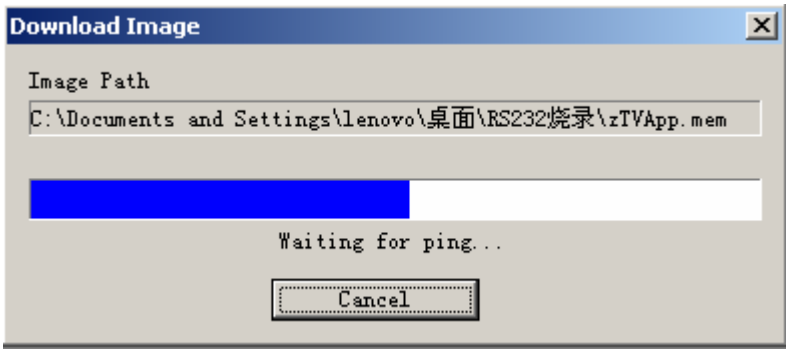
Step 3: Flash only the file required





Step 5: Press reset or cycle the power from the Evaluation Board and click “down”





Step 6: View hex file flashing progress, after the files have been downloaded, Click “Close” to exit

8、Software Platform Reference TV Application

8-1 Introduction

This document describes Phobos's reference TV application, supporting the basic control functionalities required to watch television. The reference application is designed to assist Phobos customers inimplementing a DTV system, using the Generation9-Elite IC and its APIs. This reference application is intended to support U.S. based terrestrial analog/digital broadcasting(NTSC/ATSC), and includes Electronic Program Guide (EPG), closed captioning, and parental control, as well as basic TV controls and underlying A/V decoding. The reference TV application layer lies on top of Phobos's Cougar API middleware that provides the Transport/Audio/Video/graphics driver functionalities as a chip-independent set of APIs.

8-1-1 Supported Functions

The supported application functions are:

- Power control
- Source selection
- Channel change (up/down, recall and direct digit key input)
- Volume and mute control
- Closed caption selection
- Electronic program guide
- Menus: audio, video, setup, feature

8-2 The Phobos Reference TV Application

This chapter describes basic TV controls such as channel changing, source selection, and mute/volume control. These basic functionalities are made available through the combination of GUI and standardized TV APIs. The application also utilizes the results of PSIP parsing and decoding of EIA708/608 data. These are used to support closed captioning and parental control, both of which are required on television sets sold within the U.S.

In addition to **Tuner**, **AV Input** and **Channel Map** APIs, the reference application uses a set of **Control Array** APIs to control the hardware blocks. These provide a standardized way to control the various hardware blocks in the TV chassis.

8-2-1 Power Control

The current reference application does not support standby power control as part of this implementation. Instead, pressing the power button on the remote and front panel controls the display and audio outputs only. A power-on configures the system based on Control Array values stored in non-volatile memory.

8-2-2 Source Selection

The Reference platform has analog/digital baseband inputs as well as transport input through ATSC digital channel. The **TV/Input** button cycles through the input sources:

1. RF
2. Front Composite (shared with S-video)
3. Rear Composite (shared with S-video)
4. YPbPr Component 1
5. YPbPr Component 2
6. VGA
7. HDMI input

The displayed banner for changing source is the same as the channel banner, except for displaying source number and name.

8-2-3 Channel Change

There are three ways to select a channel in the reference TV application: channel up/down, digital, and last buttons in remote controller.

- Pressing the channel **up** or **down** key tunes to the next highest or lowest channel in the selected channel map; a channel in a different channel group (analog or digital) is tuned at the limits of the available scan. The channel map is established through the Auto Program menu, which automatically removes any no signal channels. After channel scanning, the channels are grouped as digital channels and analog channels.
- For digital channels, the channels are sorted on the virtual channel number. Further manual editing of the channel list can be done through the Manual Channel Set menu. If no channels are enabled in the selected channel map after initial power on, then the channel up/down keys select the channel number next to the current channel, and determine the analog or digital channel based on the availability of signal.
- Channels can be directly accessed by pressing the digit keys on the remote controller. The channel selected is tuned immediately if the **OK** key is pressed, or will be tuned automatically after two seconds of inactivity following the last entered digit. If the entered digit keys starts with a zero ("**0**"), the channel number will be tuned to the second digit (for instance, the digits **03**, entered in sequence, will tune immediately to channel 3). Any channel may be selected by this method, regardless of its presence or absence in the current channel map.
- Pressing the **Last** key in the remote control tunes the channel selected prior to the currently tuned channel. For ATSC channels, it selects the sub-program number as well as the channel number.

The above channel-change operations are implemented via the **Tuner** and **Channel Map** APIs.

After tuning, the application displays the information of the currently-tuned channel. This includes:

1. Channel number [Ch 9-1]
2. Channel Label [for instance, KQED]
3. Current Time [for instance, 12:30 PM]
4. Rating information [for instance, TV-PG]

The virtual channel number will be displayed if the current channel is digital. The channel label is extracted from input signal if there is no label setting for the current channel. The channel label can be explicitly set with Channel Labels menu, which will use **TLChMapSetChannelName** to store the label.

8-2-4 Volume and Mute Control

Pressing the volume **Up** or **Down** button changes the current volume in the Control Array and applies this change to the hardware block. The range of control is determined by the Control Array; the current implementation has a range from 0 to 63. Pressing either of the volume keys clears the mute audio mode of operation, if previously set. If no button is pressed for five seconds after pressing the last volume **Up** or **Down** button, the volume display will be automatically removed.

The reference application supports audio **mute** or **unmute** by pressing the **Mute** key. When mute is enabled, the audio is muted, displaying an icon on upper right side. The mute condition is cleared when the TV is powered off.

Pressing the **Mute** key invokes the mute icon on the right corner of screen.

8-2-5 Closed Caption Selection

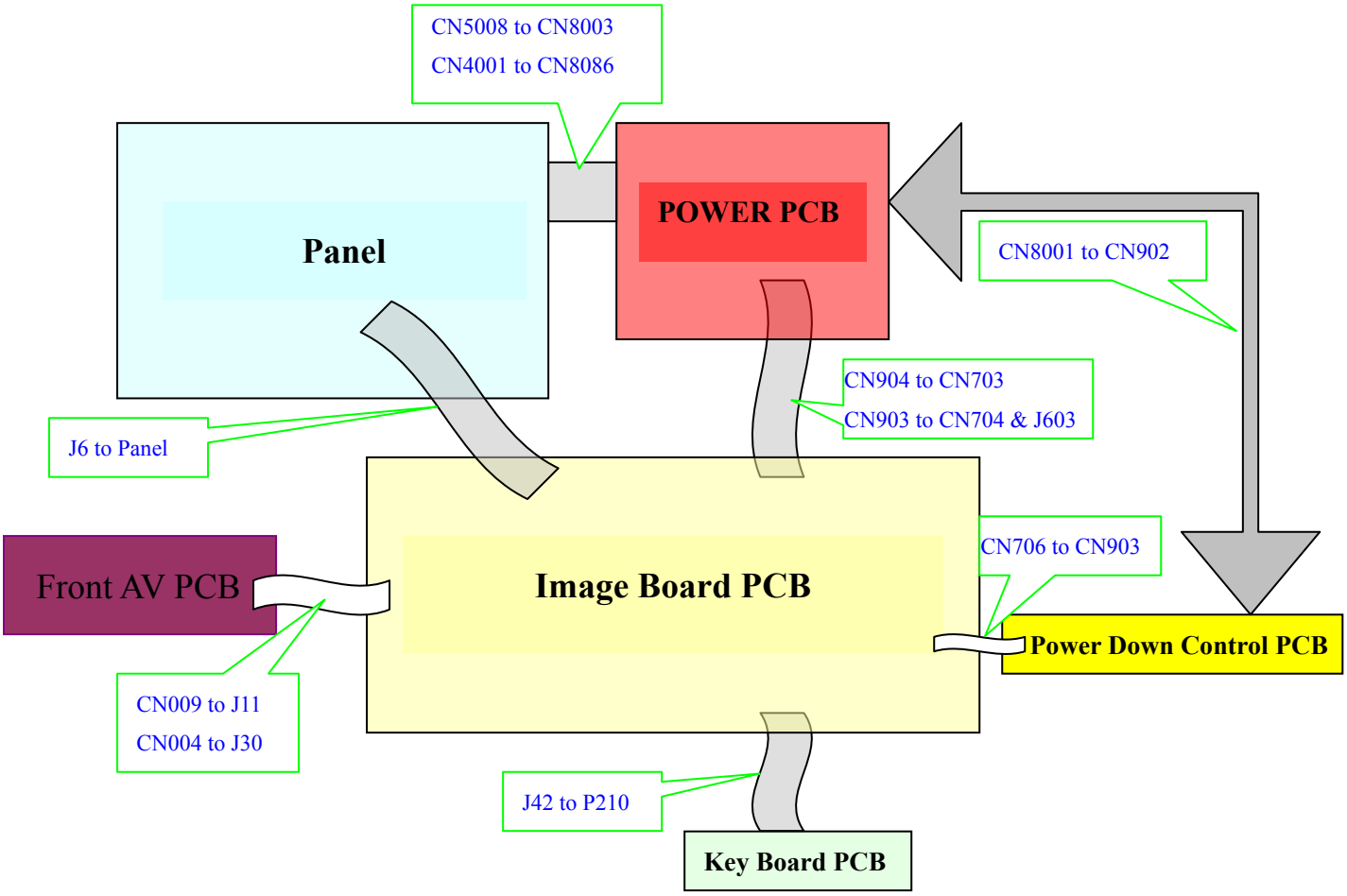
This section describes how to enable **Closed Caption** (CC) on the Phobos TV application. When the TV is switched ON, captions are disabled by default. The user switches captions ON using the **[SUBTITLE]** key on, a new language/CC option is displayed near the bottom center of the display. The sequence of options available are listed below (depending upon the stream type- ATSC/NTSC).

For ATSC, **English – Spanish – French –Portuguese-Off**

For NTSC, **CC1 – CC2 – CC3 – CC4 – Off** The displayed CC option can be set either, it is set automatically after two seconds.

9、Block diagram & Explain

9-1 PDP block diagram and functions



Function of Board:

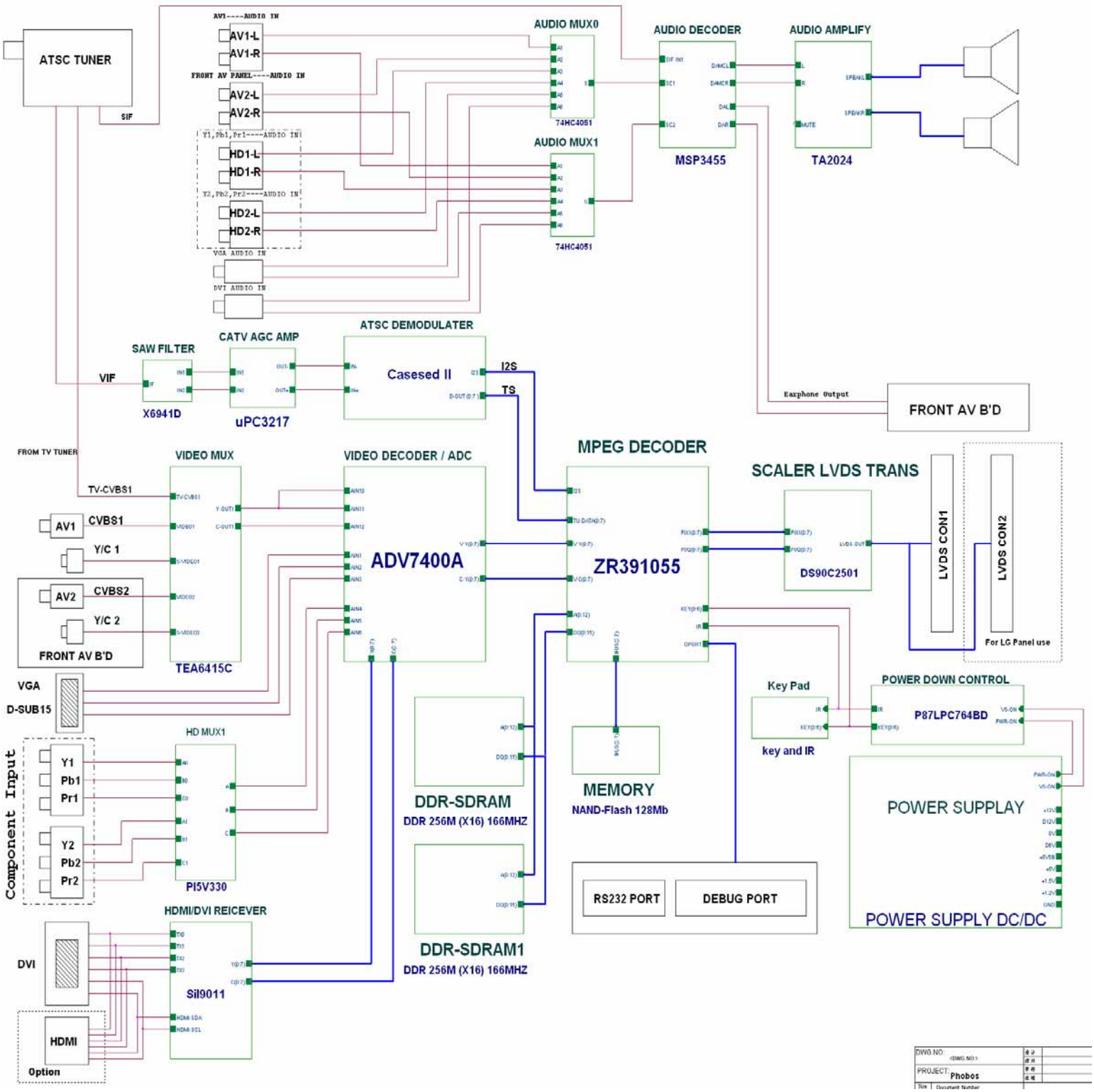
1) IMAGE Board : Control all input signals, Decode the video signal, De-interlace, and send digital signals (LVDS signal) sent from image Board and display
2) PDC Board: Power Down Control Board
3) SIDE AV Board: The input signal interface
4) Power Board: Supply Power for Panel and Image Board
5) KEY Board: POWER, Signal Source, MENU, CH+, CH - / VOL +, VOL -
6) Power ON /OFF: Turn power on/off

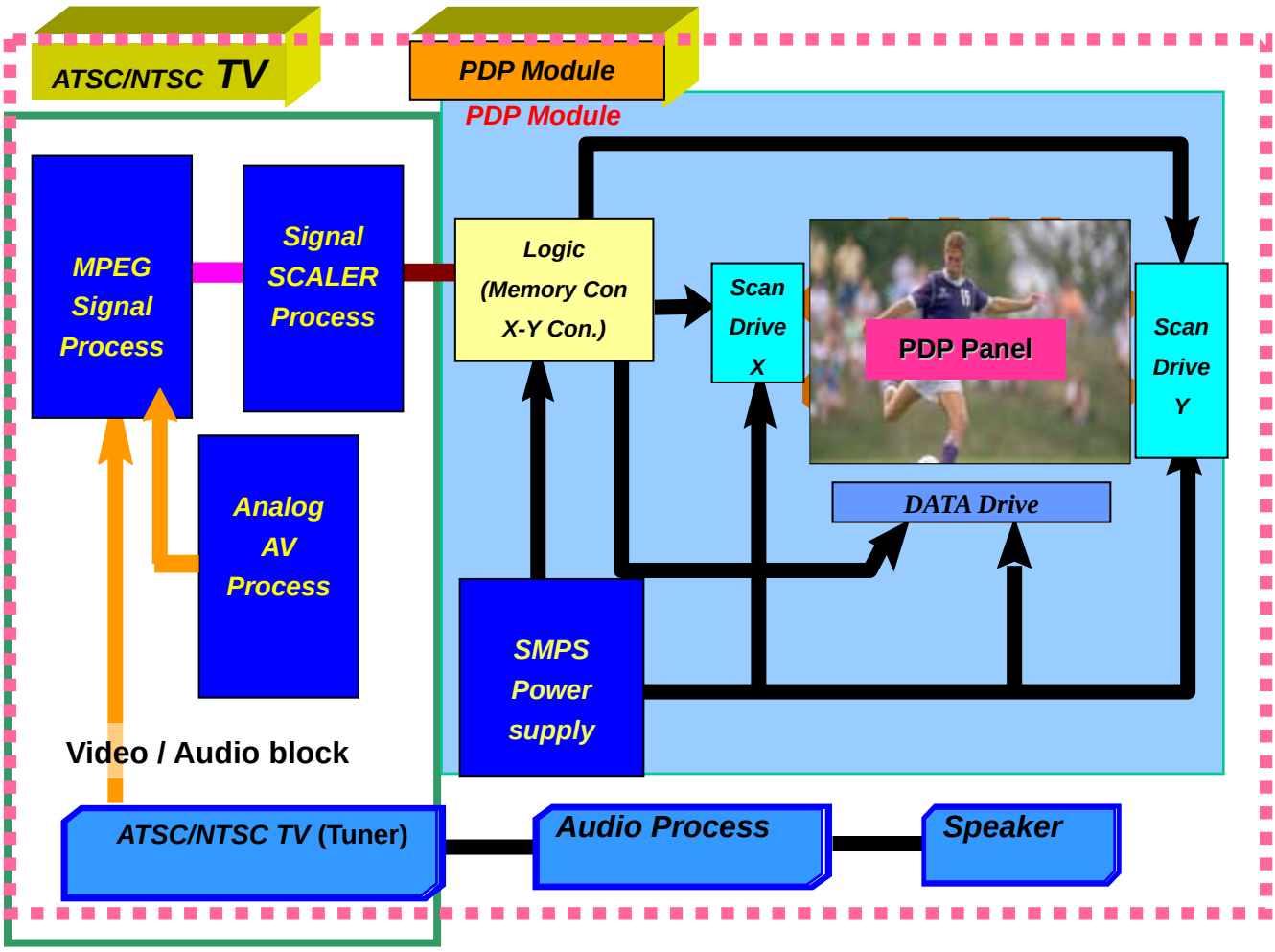
Part apt to decrease:

1) BEZEL, REAR COVER& GLASS FILTER
2) Panel
3) Terminal Board's RCA plug

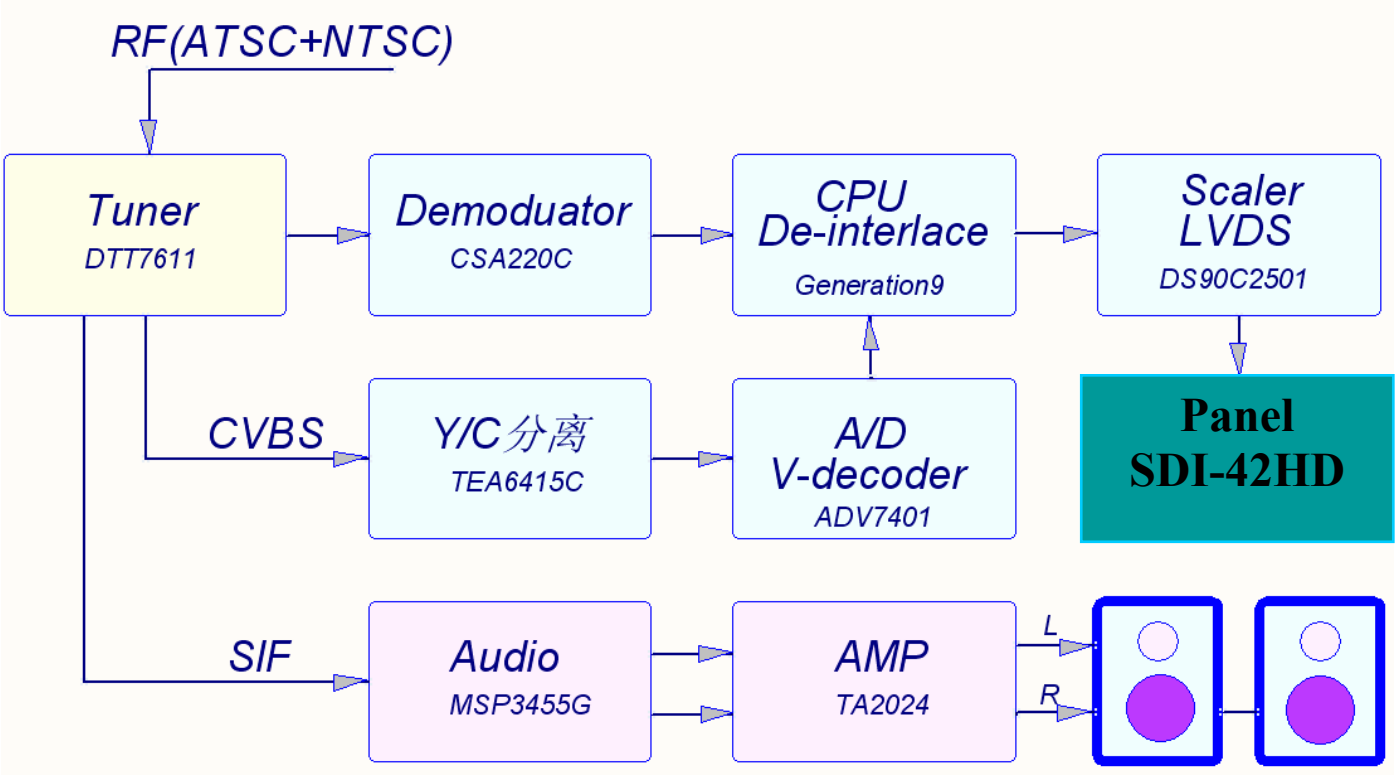
9-2 Image board block diagram and signal introduce/process

9-2-1 Image board block diagram





9-2-2 Signal introduce/process



ATSC+NTSC TV RF signal are separated into 2 way output when enter into Tuner. One is NTSC (Analog signal) that output video signal by mixing, amplifying, demodulating. Video signal are separated into Y/C signal throughTEA6415C, and transferred into ITU601 through ADV7401, then send into Video-audio process chip Generation9. Tuner output SIF audio signal to MSP3450G to process, amplify, then put in D-type amplifier TA2024.

The other ATSC (Digital signal, ATSC channel bandwidth is 6MHZ) via Tuner transferred into TS-stream through 44MHZ intermediate frequency amplify, ASW filter, QAM\OFDM demodulate, then enter into Generation-9 to MPEG decode, video part revert into video signal through coding, and transferred into double-field TTL signal by this chip process. Then put into Scaler and LVDS drive chip DS90C2501, through coding output 5 pair LVDS signal to drive PDP panel module. Digital audio signal from Generation-9 revert into Audio signal to MSP3450G through PCM decoding.

Program information in TS-stream be parsed and stored, user could know related program information through OSD query menu. For multi-program TS-stream, user could appoint to see some program in this stream through program guide EPG.

AV, S-video, YPBPR, DVI, D-Sub and each Audio signal through two group of 74HC4052 switch with ATSC audio signal together put into MSP3450G, through alt, woof, balance, volume, SRS, BEE process, then amplify by D power amplifier TA2024,output to loud-speaker.

9-2-2 Input signal introduce

1. VIDEO: transmit bright & chroma signal , it is general ,its picture quality is equal to the general VCD.
S-VIDEO transmit the bright and the chroma single, and can reduce/control the cross-interfere , it is better than the Video.

2. RGB&D-SUB(Pc interface): general RGB simulative input interface .

3. YCbCr(NTSC/PAL): is composed of one bright and two chromatism signals U/V. due to the eye is more sensitive for bright than chroma , RGB via the formulae Y=0.39R+0.50G+0.11B to transform into one bright and two chromatism signals U(R-Y), V(B-Y).

4. VIDEO、S-VIDEO、YCBCR: the frequency 15.6KHZ 50(PAL)/60HZ(NTSC), interleaved simulative signal.

5. YPbPr: non-interlaced signal, belong to DTV scope, support 480P,720P,1080i format, current is NTSC.

6. DVI：digital Visual Interface, has 29pin（DVI-I）and 25pin (DVI-D), now many top grade display card own it.

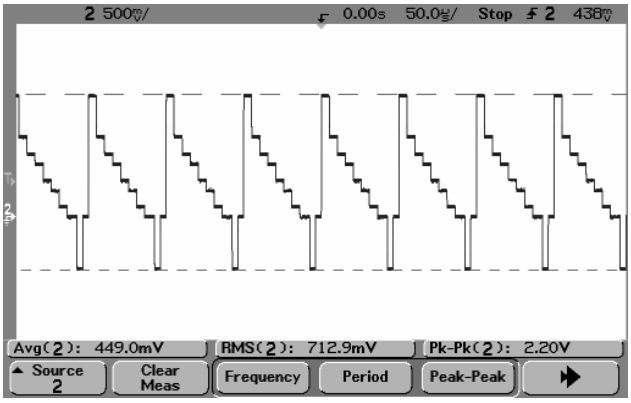
10、Waveform of signal

10-1 Waveform of input signal

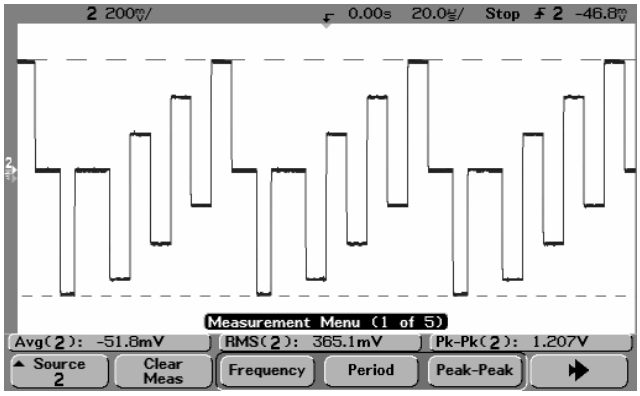
(Instrument outputs the sub board signal，Instrument：VG828/ TG19CC/Oscillograph)

YCbCr: Timing946 Pattern946 color bar picture

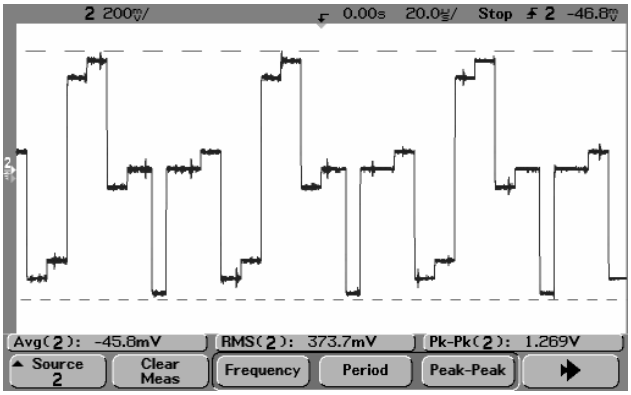
Y Luminance Signal



R Red Signal

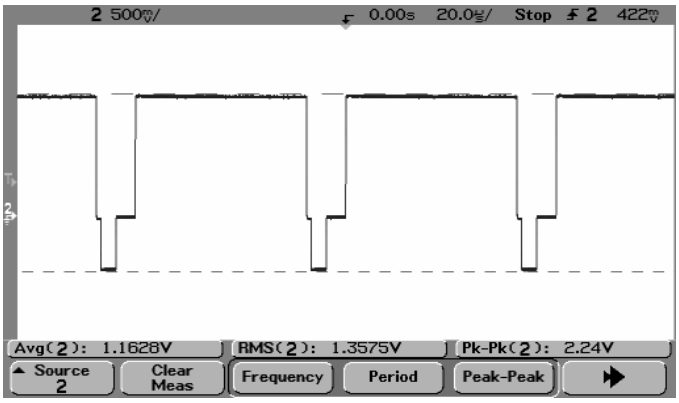

2 200mV/ 0.00s 20.0ns/ Stop 2 -46.8mV
Measurement Menu (1 of 5)
Avg(2): -51.8mV RMS(2): 365.1mV Pk-Pk(2): 1.207V
Source 2 Clear Meas Frequency Period Peak-Peak

B Blue Signal



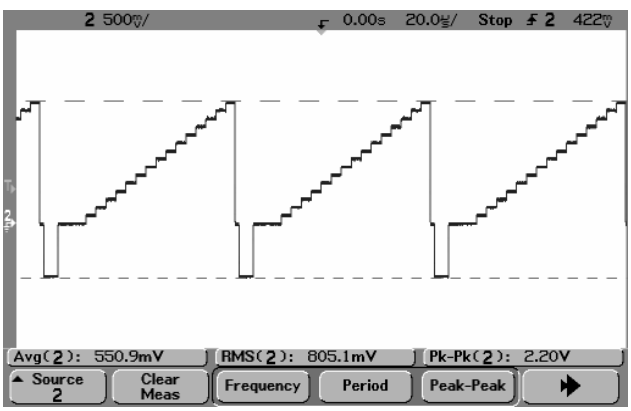
YCbCr: Timing 949 Pattern936 Full White Picture

Y Luminance Signal



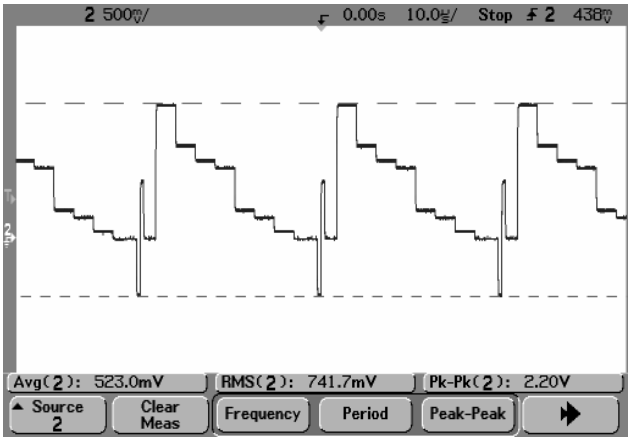
YCbCr: Timing 949 Pattern921 Gray Picture

Y Luminance Signal

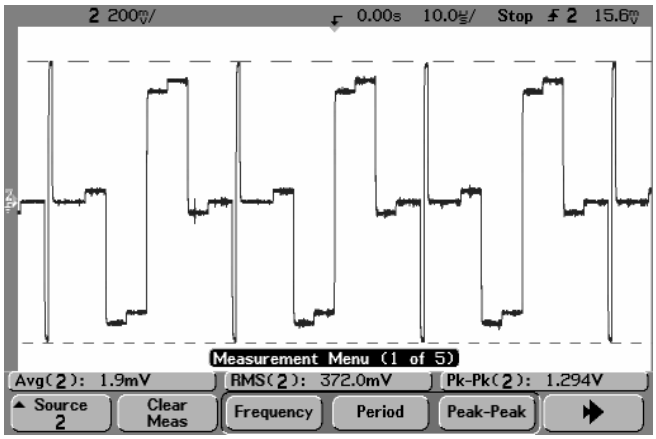


YPbPr: Timing955 Pattern946Color Bar Picture

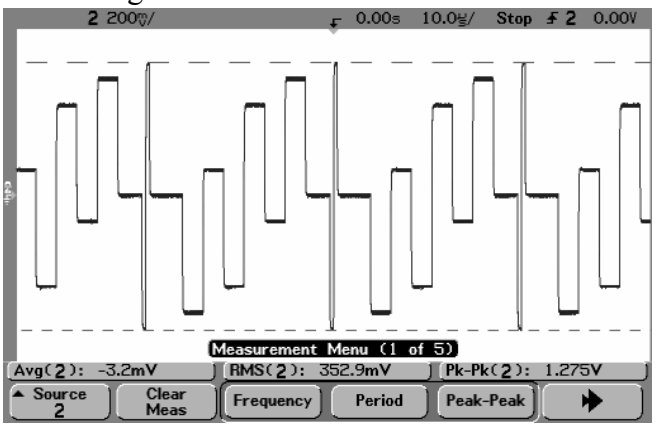
Y Luminance Signal



R Red Signal

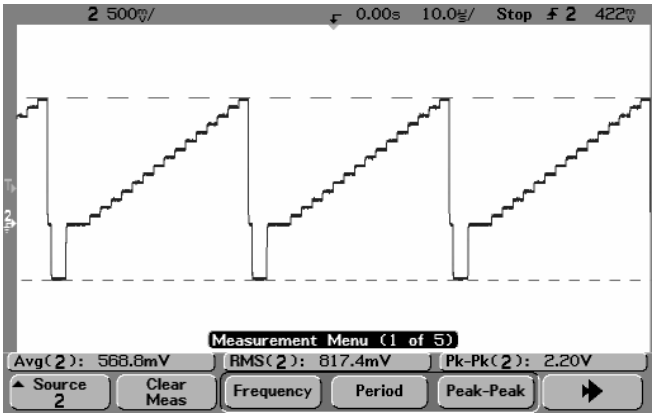

2 200mV/ 0.00s 10.0ns/ Stop 2 15.6mV
Measurement Menu (1 of 5)
Avg(2): 1.9mV RMS(2): 372.0mV Pk-Pk(2): 1.294V
Source 2 Clear Meas Frequency Period Peak-Peak

B Blue Signal


2 200mV/ 0.00s 10.0ns/ Stop 2 0.00V
Measurement Menu (1 of 5)
Avg(2): -3.2mV RMS(2): 352.9mV Pk-Pk(2): 1.275V
Source 2 Clear Meas Frequency Period Peak-Peak

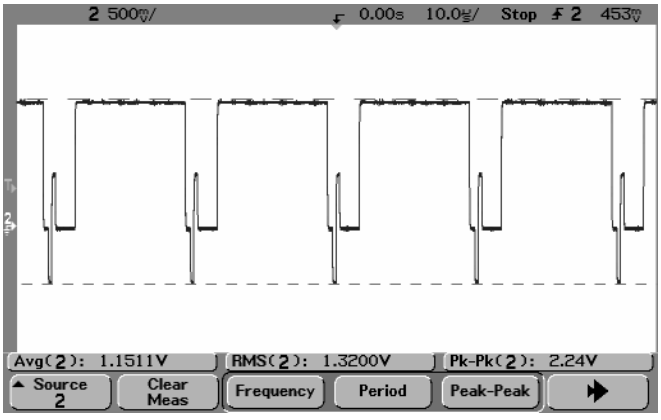
YPbPr: Timing953 Pattern921 Gray Picture

Y Luminance Signal

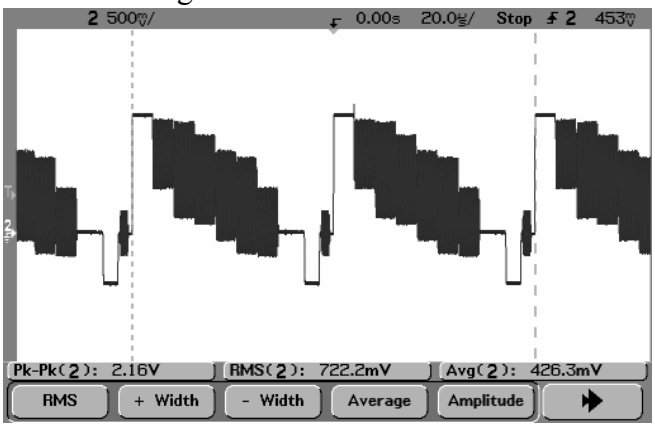

2 500mV/ 0.00s 10.0ns/ Stop 2 422mV
Measurement Menu (1 of 5)
Avg(2): 568.8mV RMS(2): 817.4mV Pk-Pk(2): 2.20V
Source 2 Clear Meas Frequency Period Peak-Peak

YPbPr: Timing954 Pattern936 Full white picture

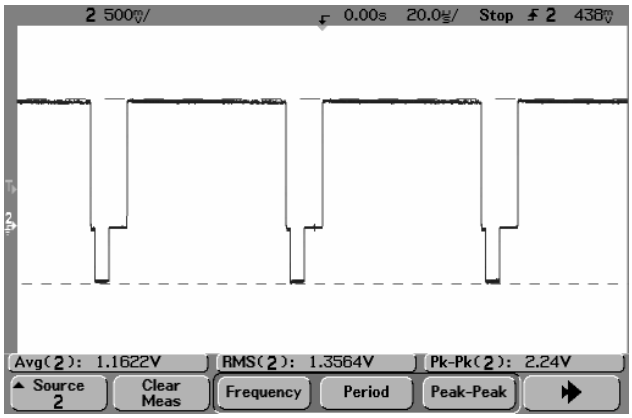
Y Luminance Signal



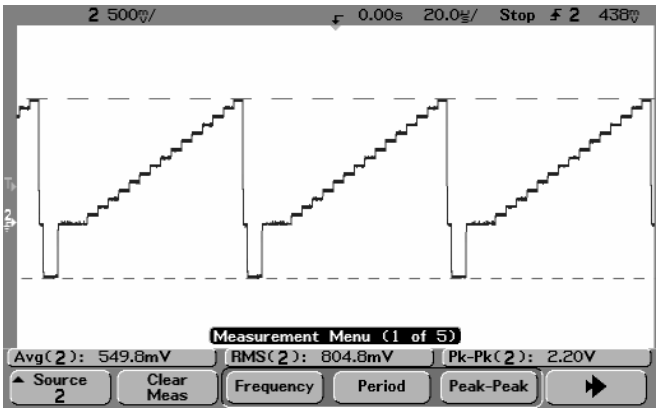
Video: Timing946 Pattern946 Color Picture



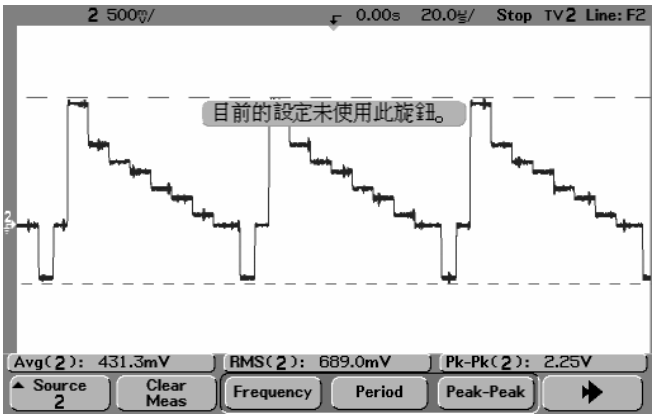
Video: Timing949 Pattern936 Full White Picture



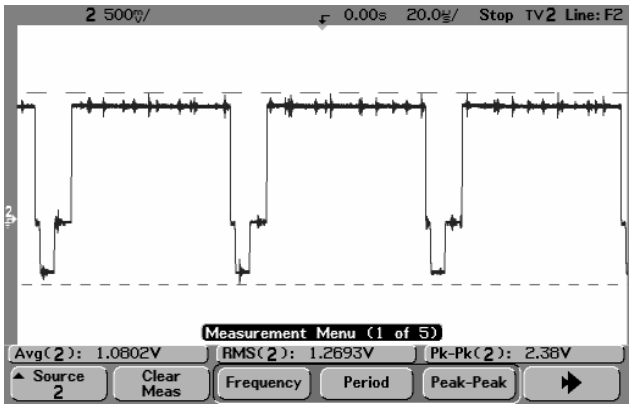
Video: Timing949 Pattern921 Gray Steps Picture



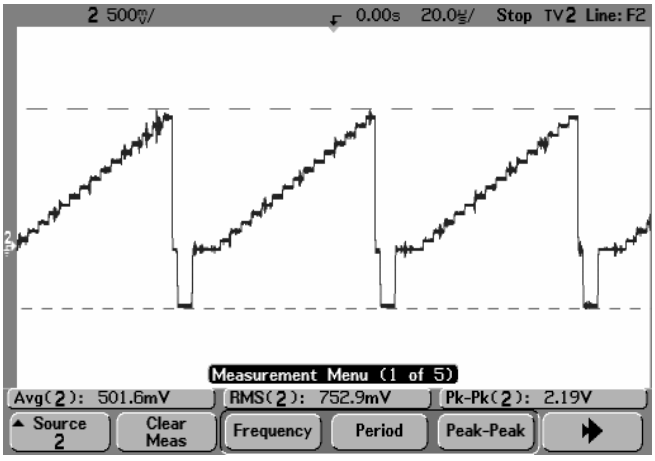
S-video: Timing946 Patern946 color bar picture



S-video: Timing949 Pattern936 Full white picture



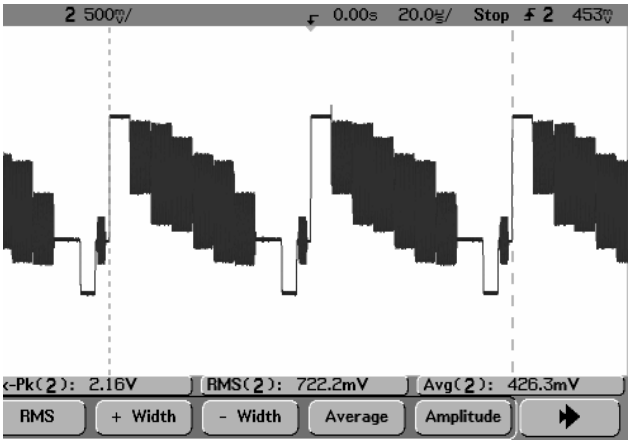
S-video: Timing949 Pattern921 gray steps picture



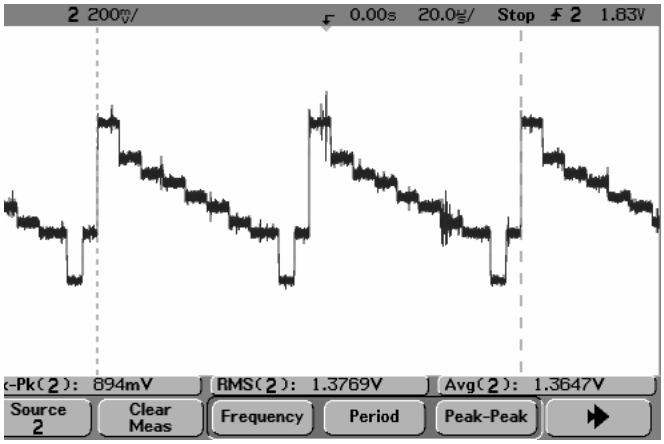
10-2 Signal waveform in the image board

Video: Timing946 Pattern946 color bar picture

U14（Y/C separate）In (pin3 C136)/(pin20 C142)

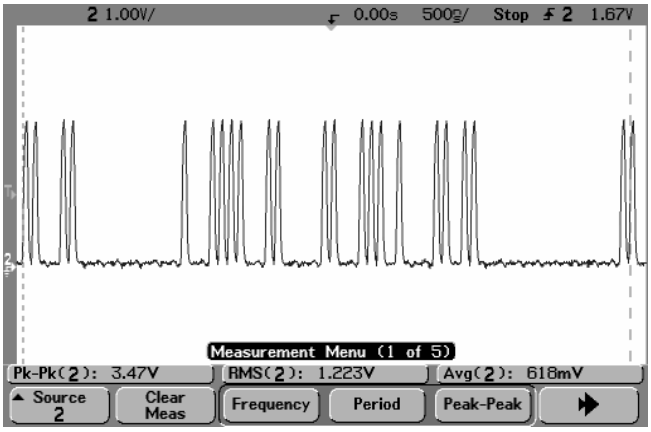


U14（Y/C separate）Out pin18/17 R119/R120



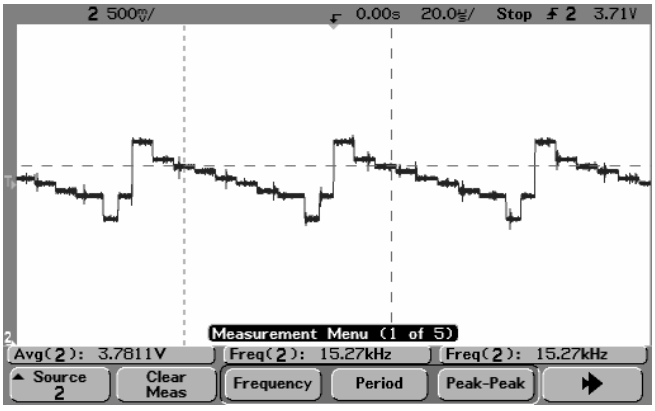
Video: Timing 949 Pattern936 white picture

U7 decoder output 8bit digital signal:



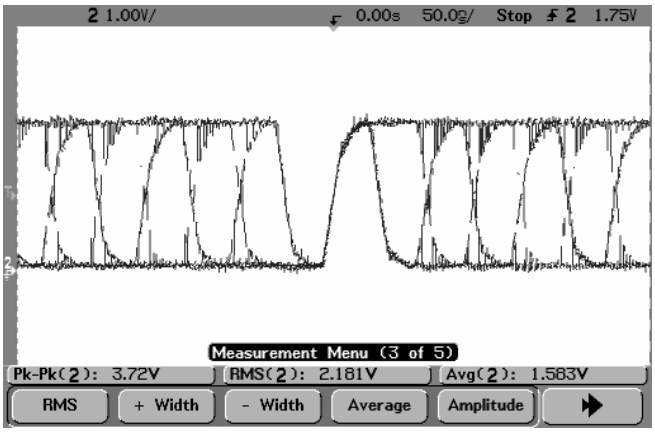
S-Video: Timing 946 Pattern946 color bar picture

U14 pin8, pin10



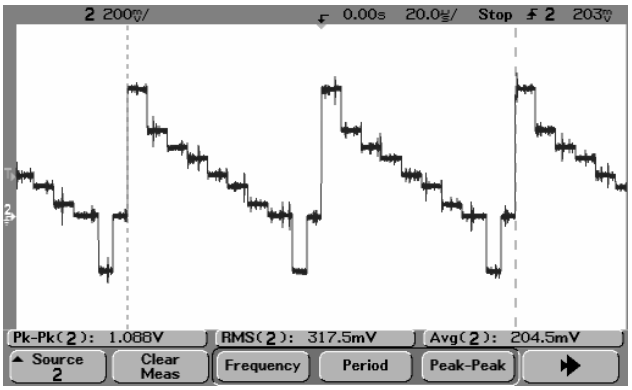
S-Video: Timing 949 Pattern946color bar picture

U7 8bit digital signal output:

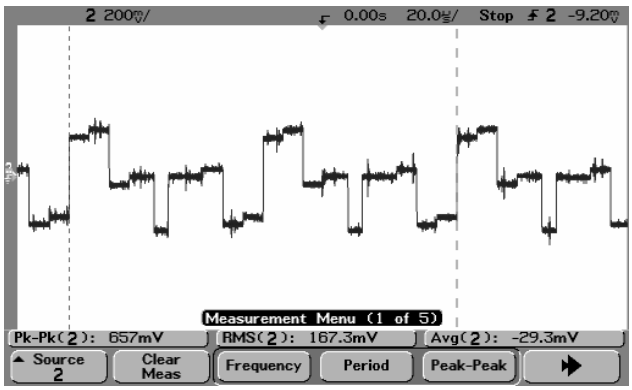


YCbCr: Timing946 Pattern946 Full white picture

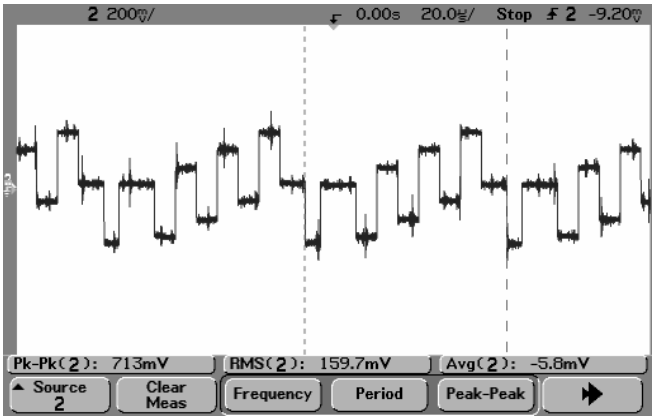
Y signal—L55



R signal—L53

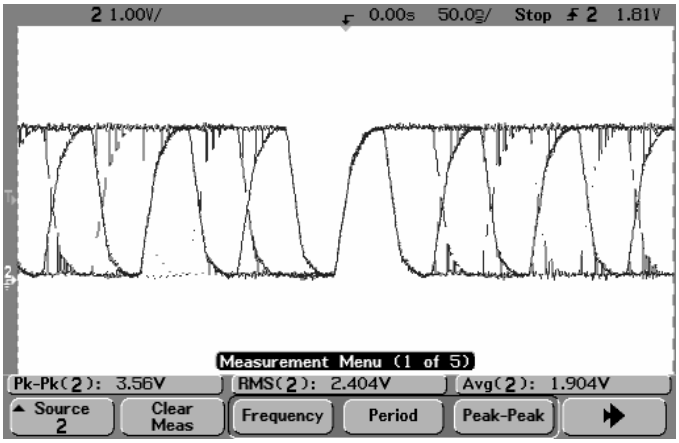


B signal—L54:



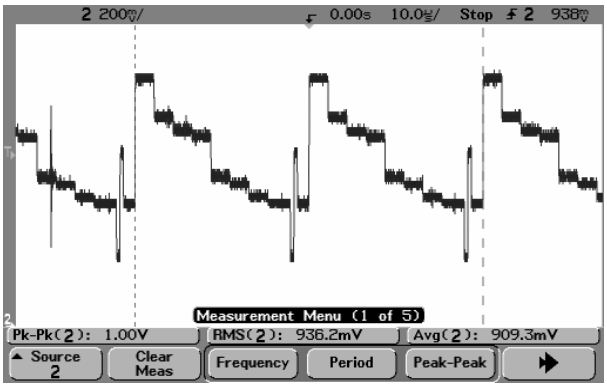
YCbCr:Timing 949、946 Pattern921、936、946 gray scale, color bar, white picture

U7 decoder output 8bit digital signal waveform

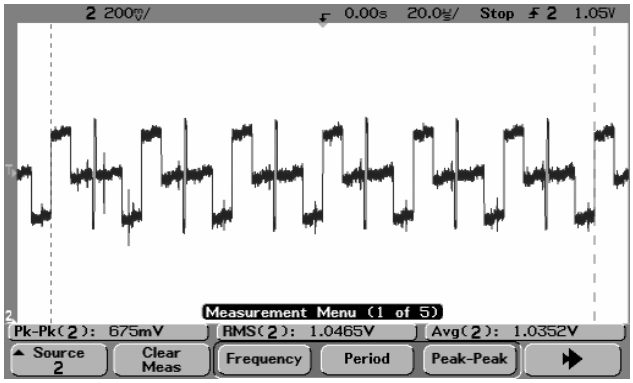


YPbPr: Timing 955 PATTERN946 color bar picture

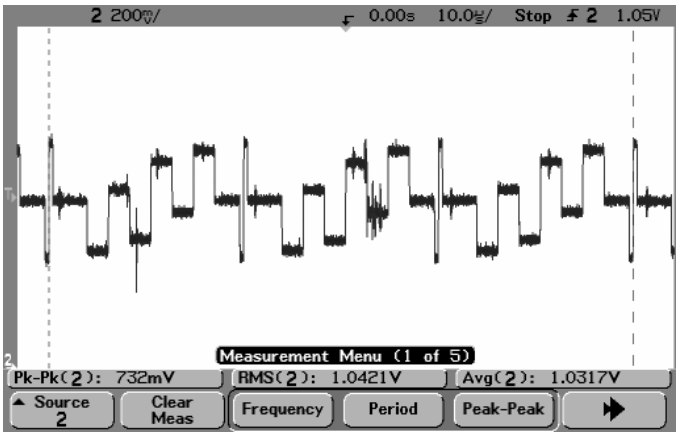
Y signal—L55



R signal—L53



B signal—L54

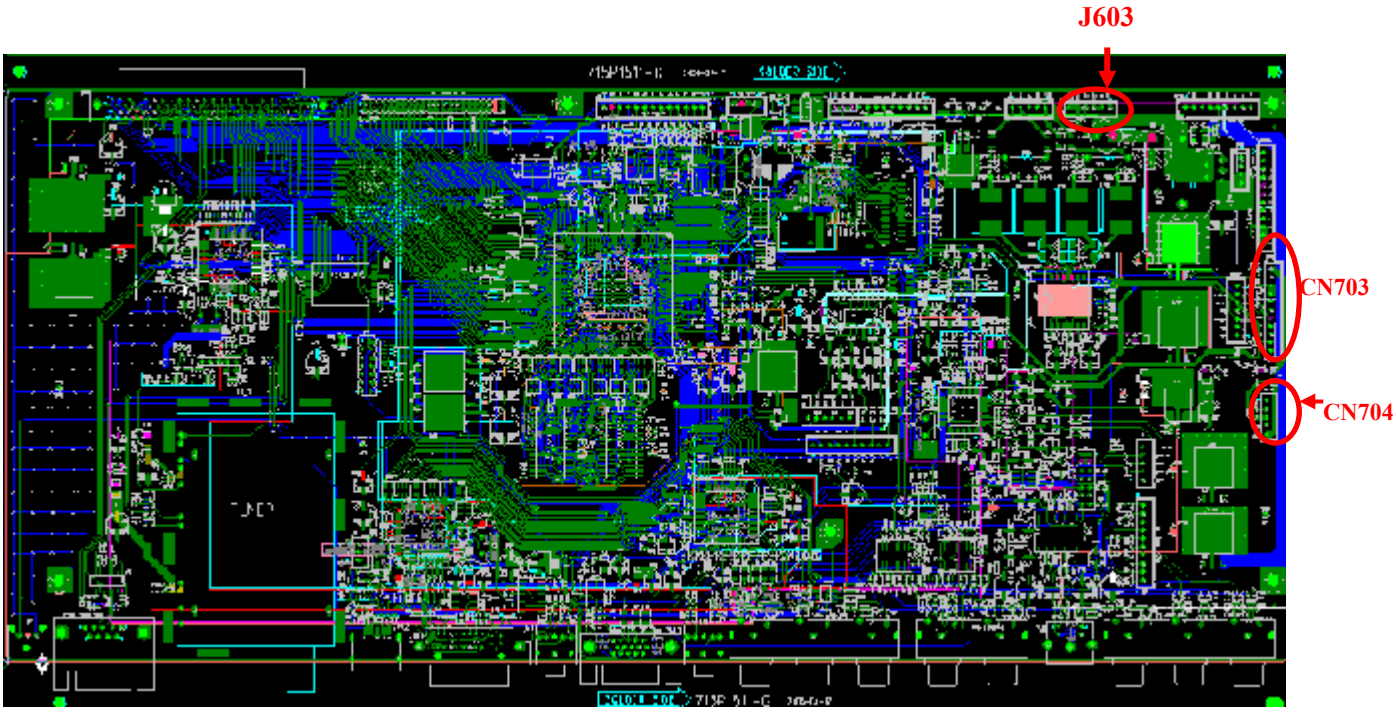


11、Check and Measure

11-1 Image board

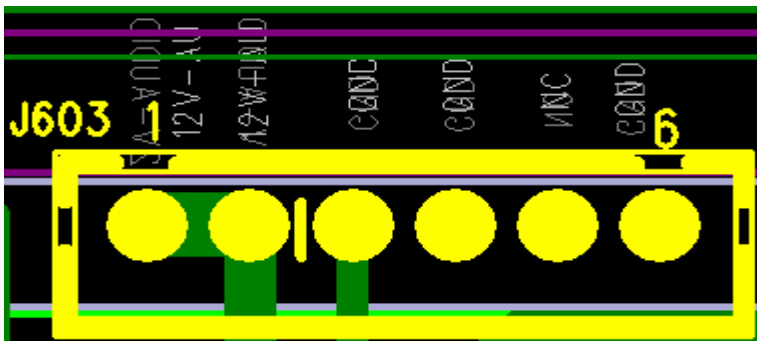
Test the power of each chip with the universal meter, to ground impedance and earth situation.

11-1-1 Power Check and Measure

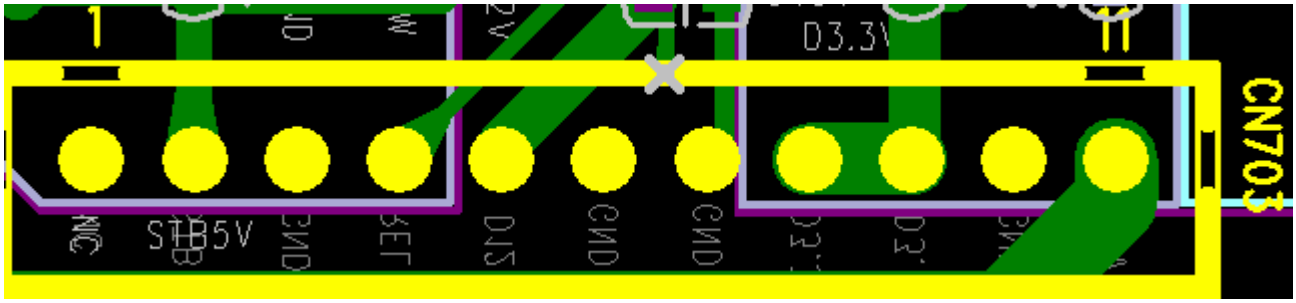


Supply with getting red arrow point three interface J603, CN703 and CN704 that identification come out for power, image of board with the interface among having picture, it corresponding power make detection method separately among following several picture. :(Only for SUMWUNG POWER)

①. In the following the first picture it is successively 1 to 6 pin of J603 from left to right: Among them, 1pin and 2pin connect 12V voltage; 3pin, 4pin and 5pin are digital earth; The second picture it is 1 to 5 pin of CN704 from left to right: Among them,2pin and 4pin of CN704 connect digital earth, 1pin of CN704 connect D6V voltage, 3pin of CN704 connect D12V voltage ,The following picture shows:



②. In the following picture it is successively 1 to 11 pin of CN703 from left to right. Among them, The second pin connects STB5V，3pin 、6pin 、7pin and 10pin are grounded digitally, 5in connect D12V voltage, 8pin and 9pin connect D3.3V voltage,11pin connect D6V voltage .The following picture shows:

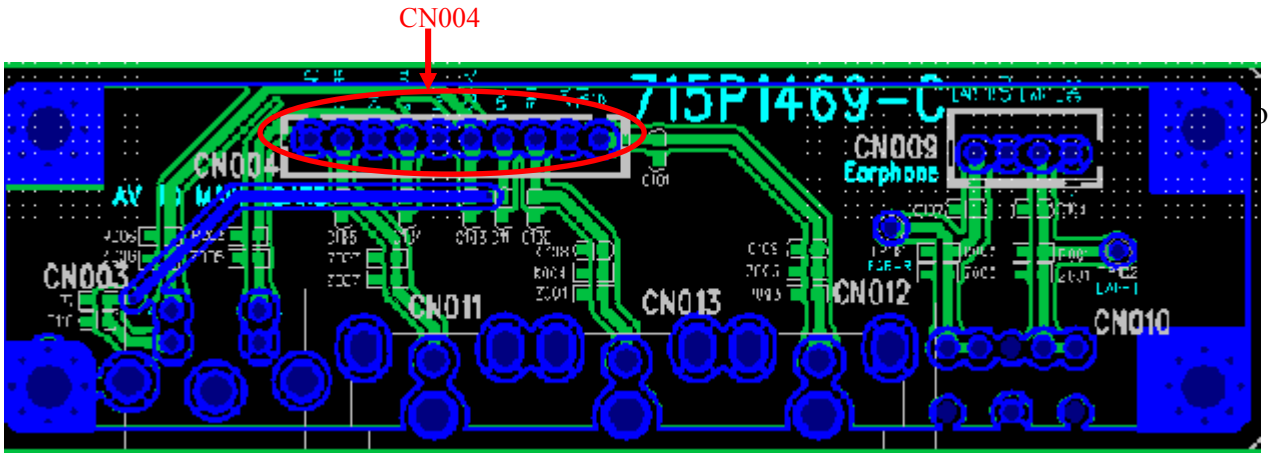


11-1-2 Voltage value of IC necessary

Voltage	Corresponding IC position and pin	
3.3V	U706 Pin3; U704 Pin3; U710 Pin3; U2 Pin38; U9 Pin13; U13 Pin3; U10 Pin91;	D40 Pin5; D41 Pin5; U68 Pin3; U30 Pin3, Pin1; J32 Pin7; U48 Pin26; U52 Pin20
STB5V	CN703 Pin2; E708; R301; R635; R68	
5V	L722,L713; L706,C718,E717; CN706(PDC Board) Pin2;	TP9; R126,R128; L216,L217; R301,R635,R638
6V	U709 Pin3; U702 Pin3; U711 Pin3;	CN703 Pin10; L703; C702
12V	J603 Pin1,Pin2; U701 Pin3; R322; L702,E711; CN703 Pin5; L701;	TP8; U601 Pin29,Pin30,Pin33; C700; U602 Pin8; U12 Pin2,Pin4; C695

11-2 SIDE AV Board

The picture below is AV SIDE board, The interface pointed out in order to provides the power for Audio board. The enlarged interface picture show in its connection.



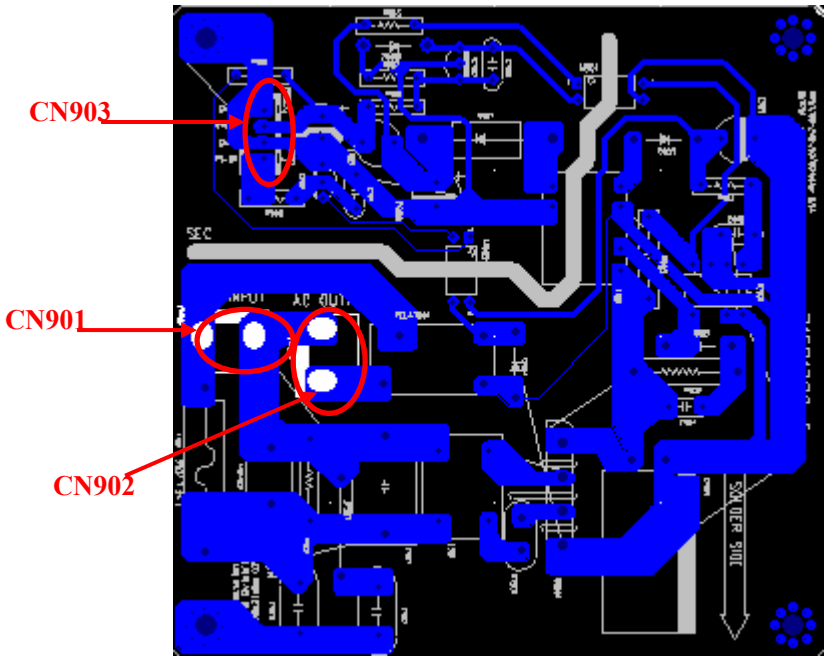
11-3 PDC Board

The following picture show PDC Board, among them getting red difference label about connection with PDC Board and main board, power board and switch of board.

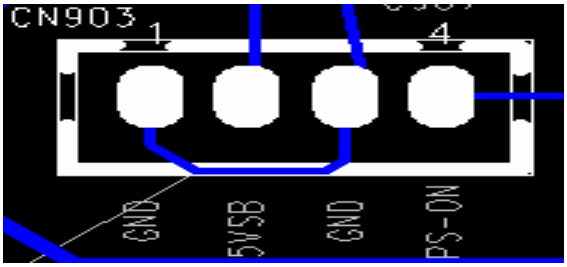
CN901: Connect with P9Z1 of Power Switch Board;

CN902: Connect with CN8001 of Power Board;

CN903: Connect with CN706 of Imager Board.

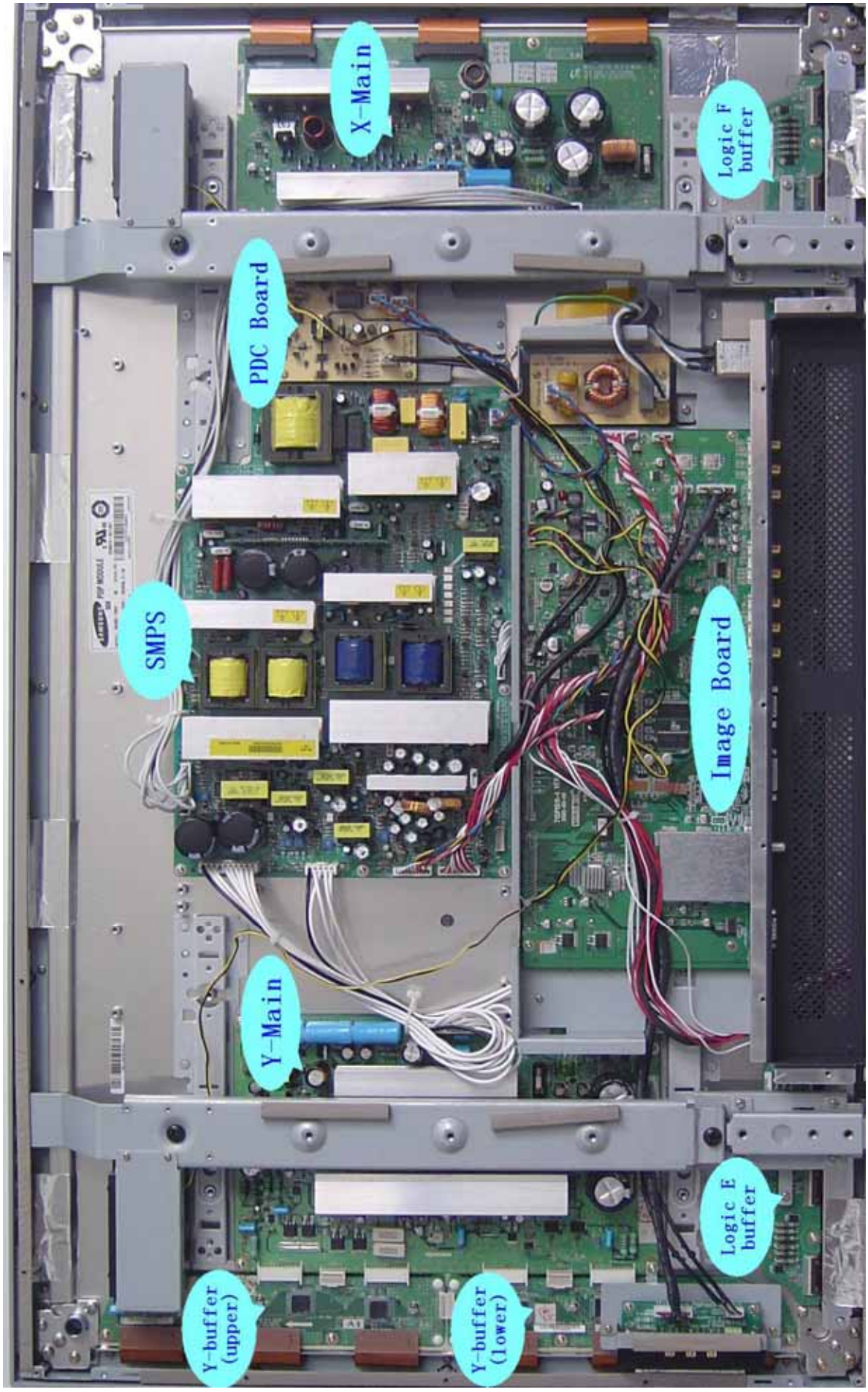


The following picture shows the pin connection of CN903:

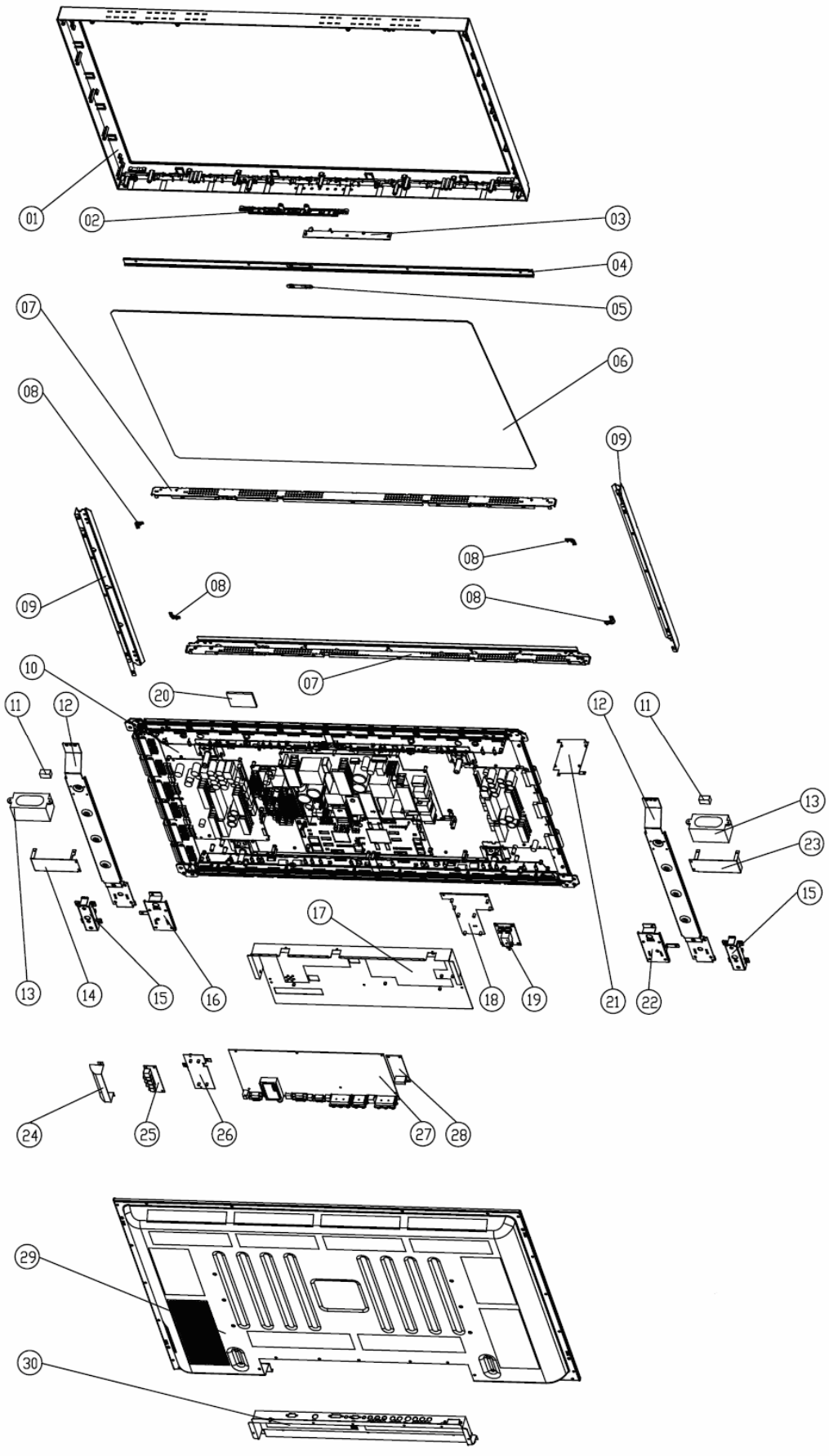


12、Mechanical Introduction

12-1 PDP Internal view



12-2 Mechanical of cabinet front disassembly



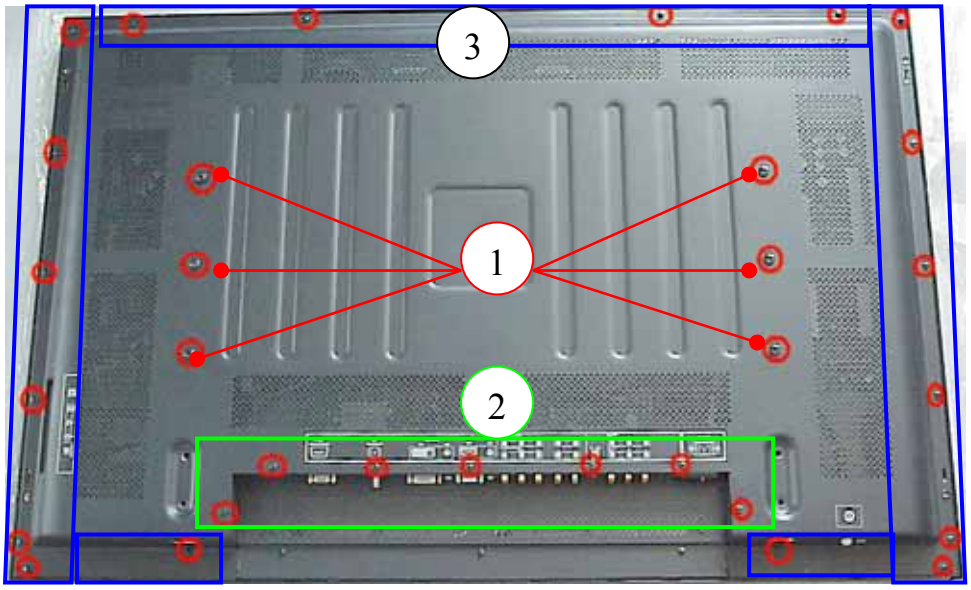
Item	Part Name	Q'ty
01	BEZEL-1	1
02	底按键	1
03	KEY BOARD	1
04	FRONT BOTTOM AL	1
05	ELNS	1
06	FIELTER GLASS	1
07	BKT SHIELD52 上下	2
08	BKT_HOLDER	4
09	BKT SHIELD-1	2
10	42" PANEL	1
11	透气泡棉	2
12	PANEL支架	2
13	Speaker	2
14	Speaker Bracket R	1
15	BKT-STAND-UP	2
16	右下支架	1
17	PCB PLATE	1
18	BKT MAIN POWER	1
19	MAIN POWER PCB ASSY	1
20	Silicone	1
21	电源PCB固定板B	1
22	左下固定片	1
23	Speaker Bracket L	1
24	Side AV cover	1
25	AV Board	1
26	Side AV Bracket	1
27	MGPC Board	1
28	滤波电源板	1
29	Rear cover	1
30	REAR LOW COVER-10	1
31	BASE-SUP-AL	1
32	BASE-STAND-ZN	2
33	BASE-SUPPOR-AL	1
34	BASE-STAND-AL	1
35	STAND-BASE-ABS	1
36	BASE-PLATE-SPCC	1
37	BASE RUBBER FOOT	2

12-3 Disassembly and assembly

12-3-1 PDP stand removal

4) Unplug the AC power and all signal cables.
5) Place the PDP upside down on a tabletop (use a protection sheet or EPE bag), Take care, that this is flat and free from obstacles like screws, to prevent damaging the fragile PDP glass filter (1).
6) Remove the four black colored screws around the stand holder (2).
7) Remove the Base assembly from PDP as the direction arrowhead showed (3).

12-3-2 Back Cover Removal



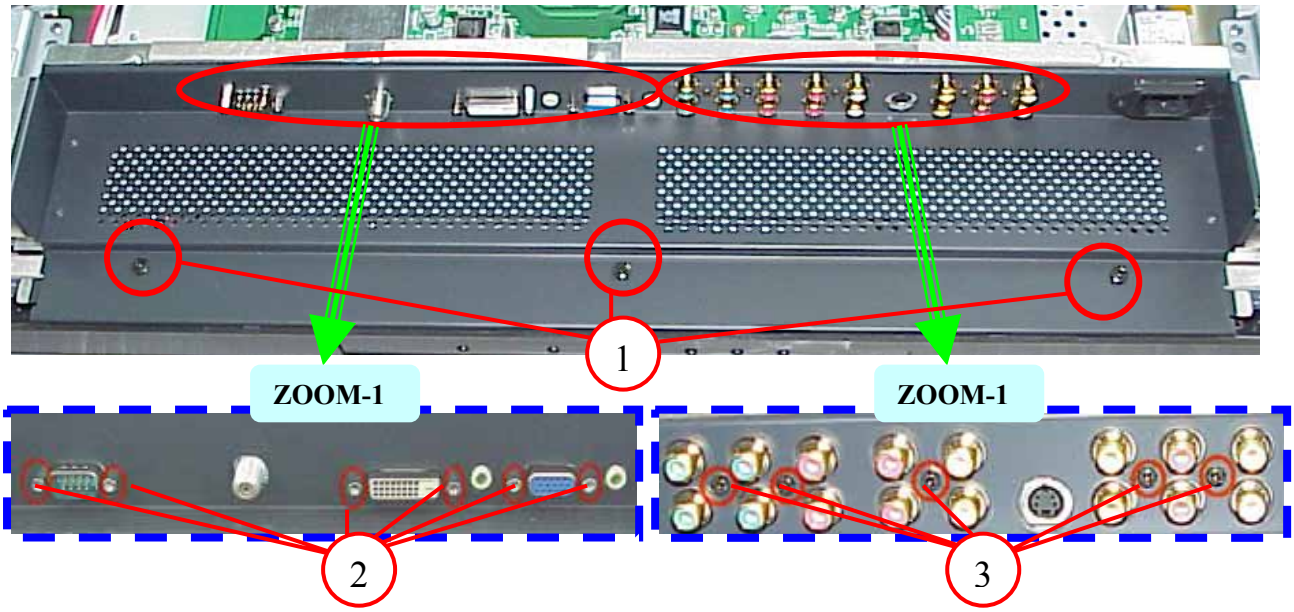
1) Remove the six big black colored screws in the panel holder as the red-circle showed (1).
2) Remove the seven black colored screws around the terminals as the green-pane showed (2).
3) Remove the eighteen black colored screws around the back cover as the blue-pane showed (3).

4) Carefully prize up the back cover from the left of the PDP (5).

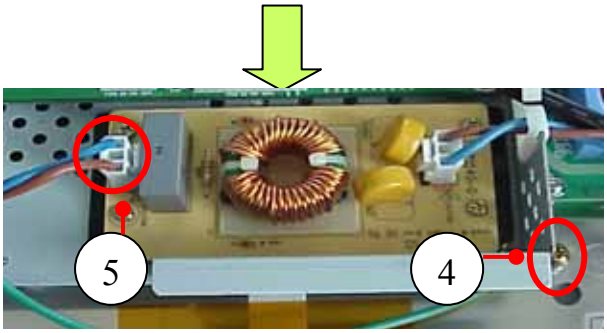
5) Carefully remove the Back Cover from the top of the PDP, and store in a safe place.

6) Done.

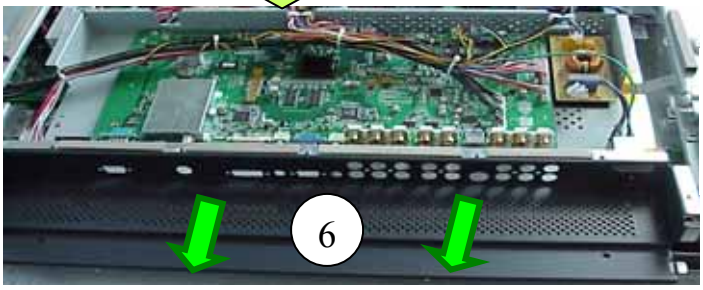
12-3-3 Rear Low Cover removal



1) Remove the three black screws in Rear low cover (1).
2) Carefully use a allen screwdriver to remove the six silver colored allen screws M3*6mm (2).
3) Remove the five black screws (3).



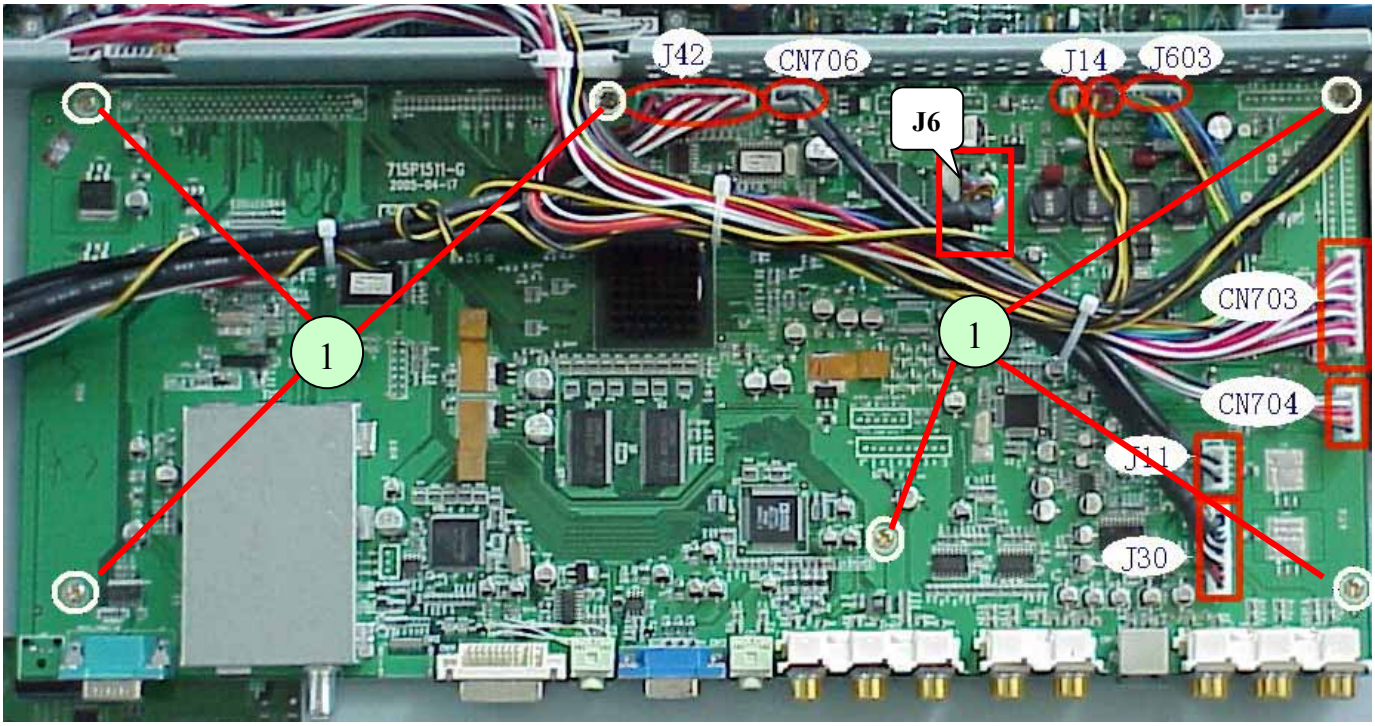
4) Remove the one silver screws and remove the GND cable (4).
5) Disconnect the AC cable from AC FILTER Board (5).



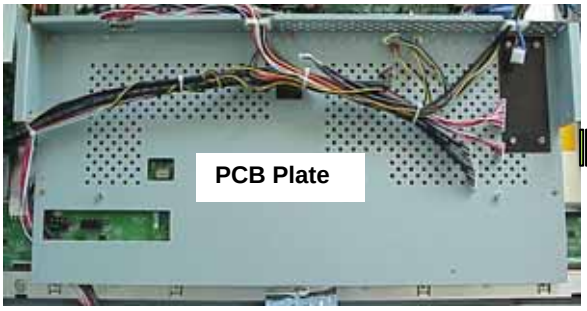
6) Remove the Rear Low Cover as the direction arrowhead showed (6).

7) Done.

12-3-4 Main Board(MGPC) removal

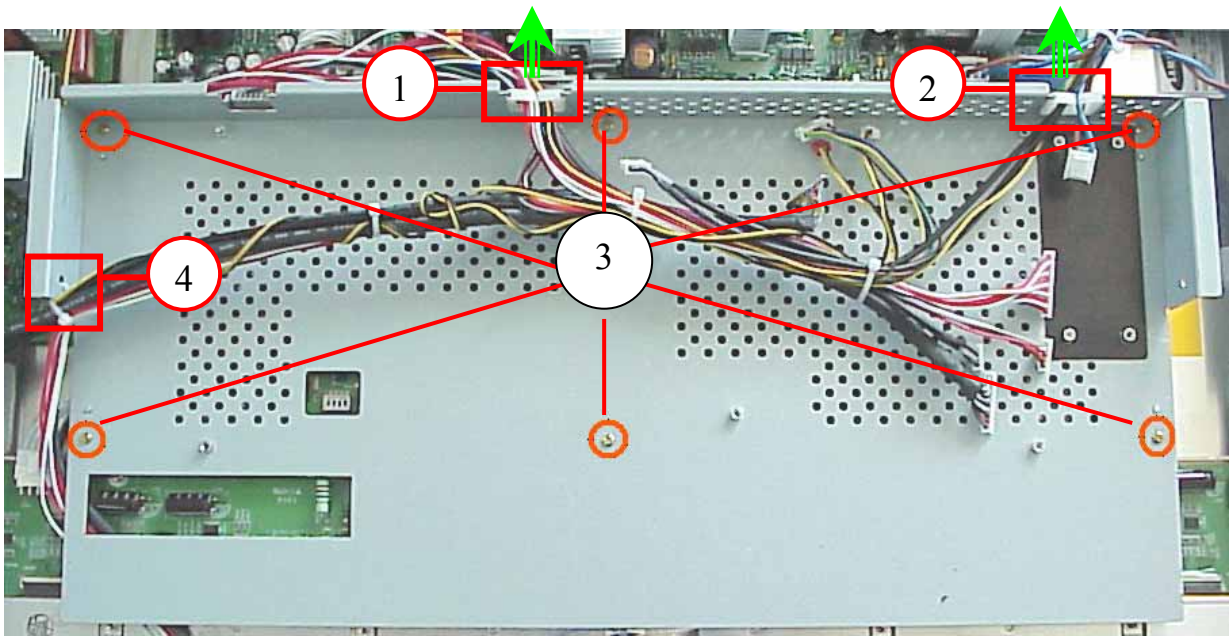


1) Disconnect the all connectors(J42,CN706,J14,J603,CN703,CN704,J11,J30 and J6 form M GPC(main board). See the above figure.
2) Remove the six silver screws from MGPC(main board)(1).



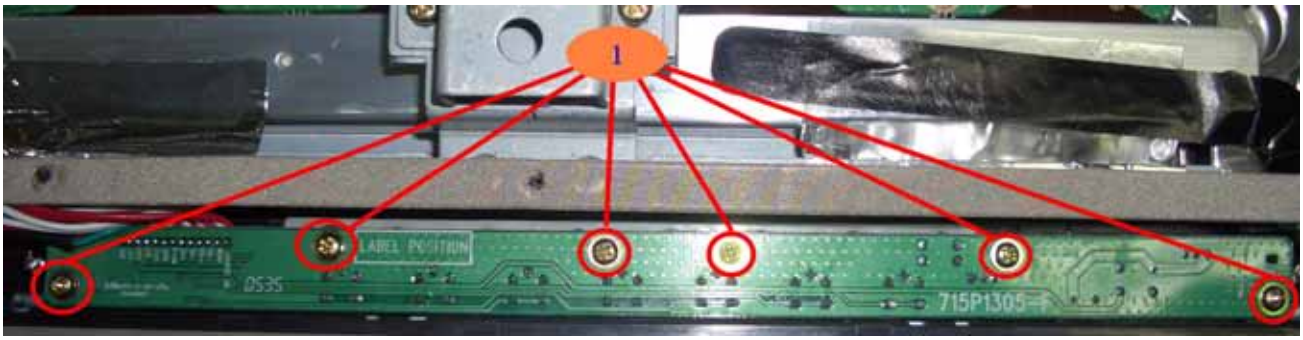
3) Remove the MGPC board from PCB plate. 4) Done.

12-3-5 PCB Plate Removal



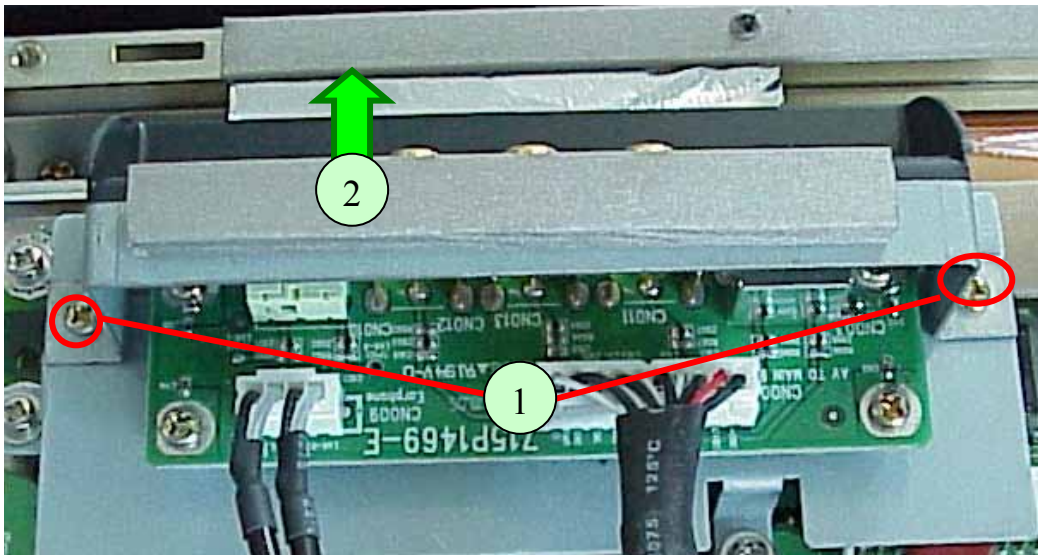
1) Remove the two Cable Clips from the PCB Plate(1)(2).
2) Remove the six sliver screws(3).
3) Cut the cable tie(4), Note, please carefully cut it, don't make the cable damage.
4) Remove the PCB Plate

12-3-6 Key Board Remove



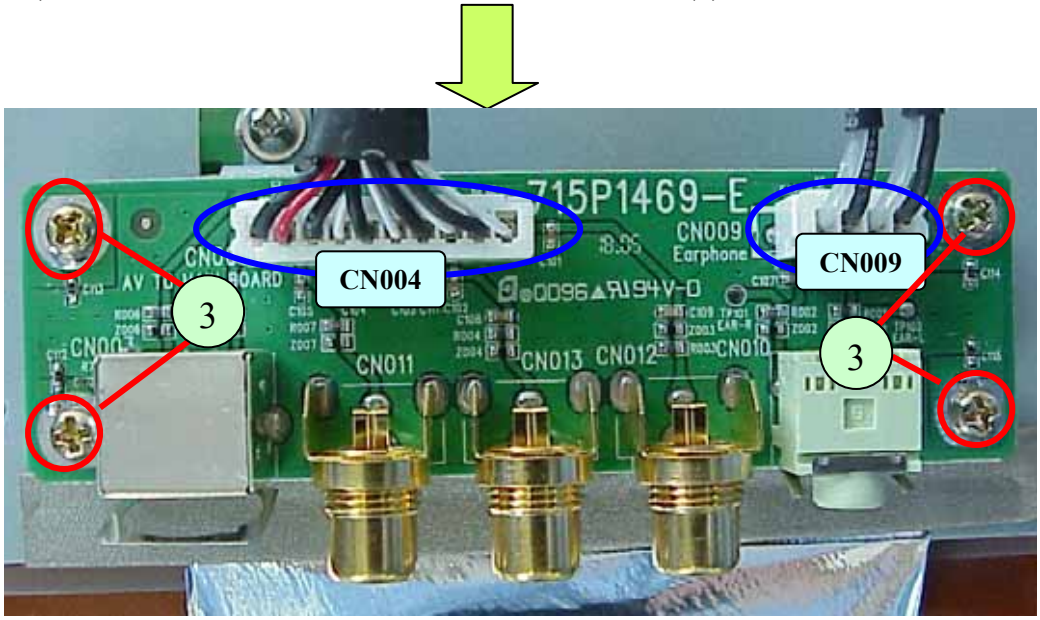
1) Remove the Six silver screws(1) to disassemble the key board from the bezel.

12-3-7 Side AV Board Removal



1) Remove the two silver screws (1).

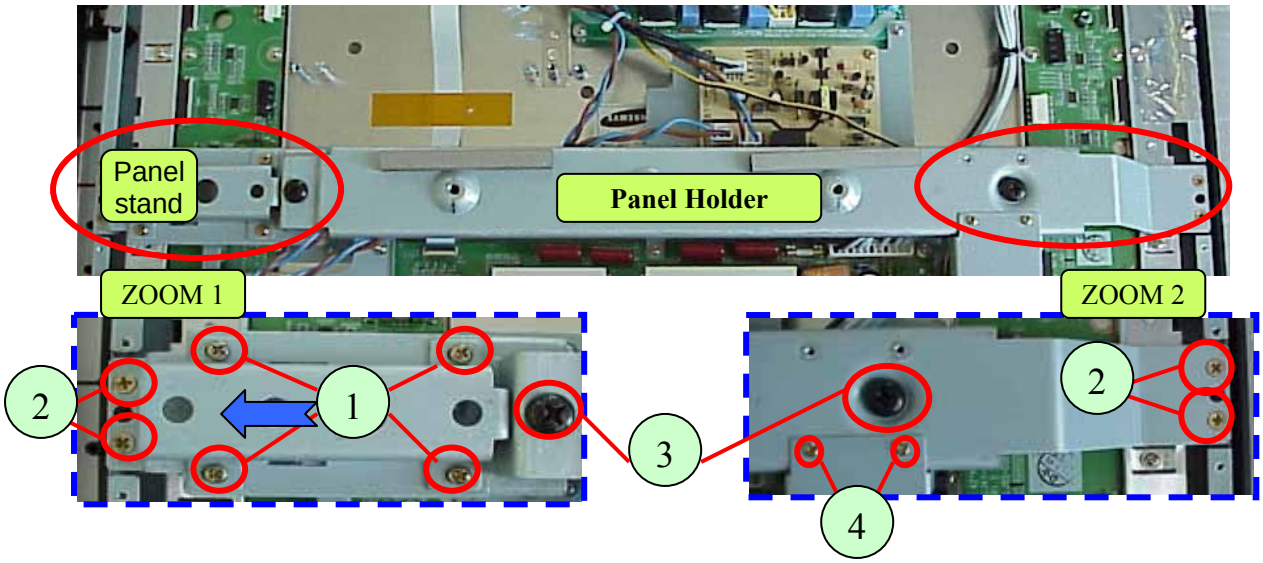
2) Remove the side cover from Side AV board(2)



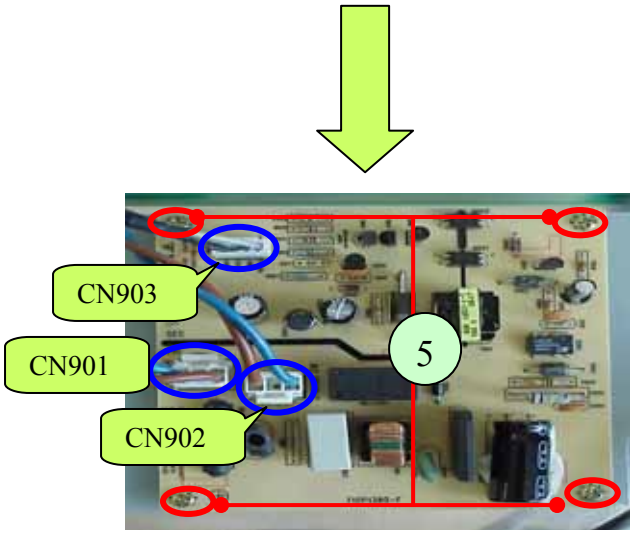
3) Disconnect the CN004 and CN009 from Side AV board.

4) Remove the four silver screws (3).

12-3-8 PDC（power down control）Board Removal

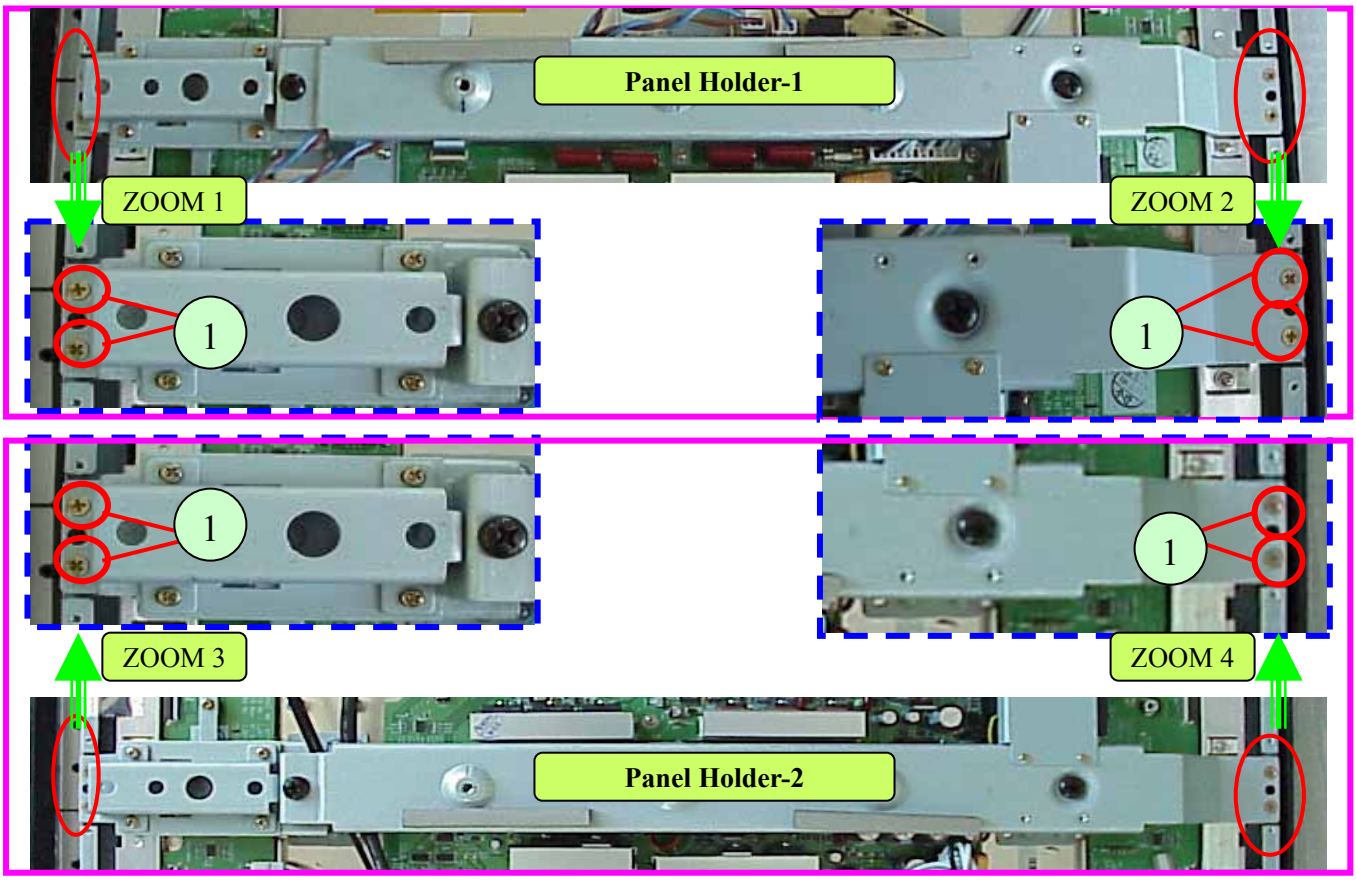


1) Remove the four sliver screws (1) and remove the panel stand from panel holder as the direction arrowed showed.
2) Remove the four silver flat screws (2).
3) Remove the two black screws (3)
4) Remove the two silver screws (4)
5) Remove the panel holder from PDP.

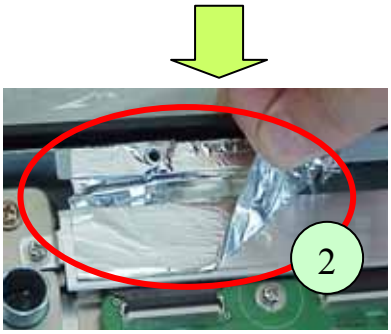


6) Disconnect CN901,CN902 and CN903 from PDC board.
7) Remove the four sliver screws (5), and remove the PDC board.

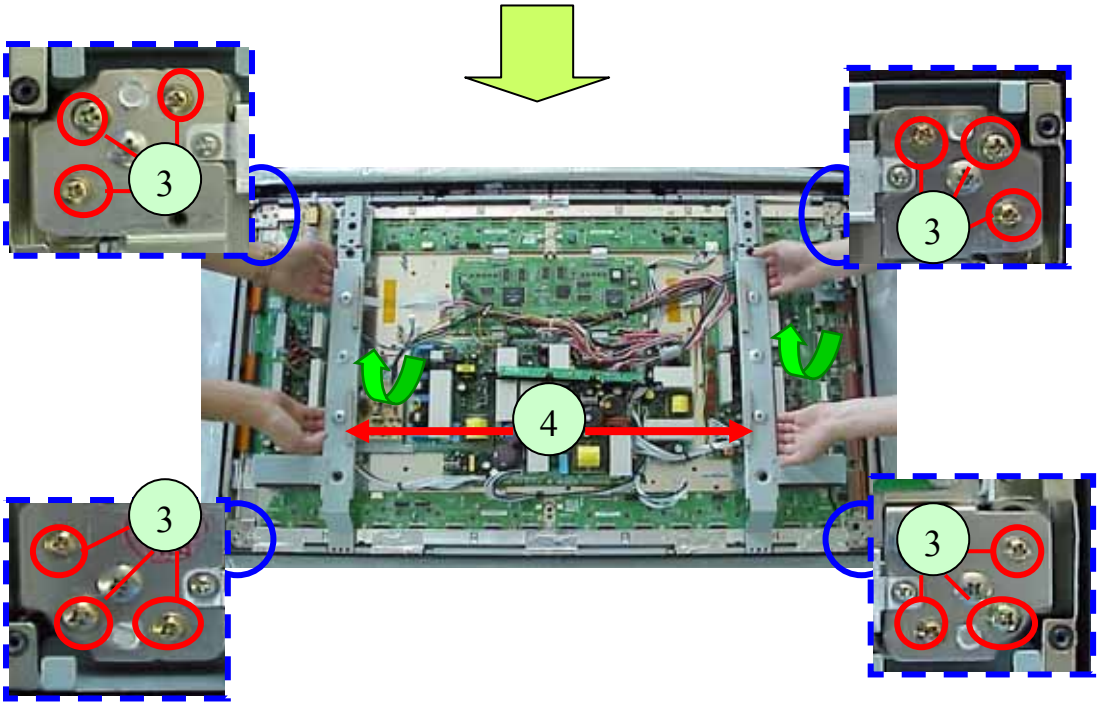
12-3-9 Panel Module Removal



1) Remove the eight silver flat screws around the two panel holder (1).

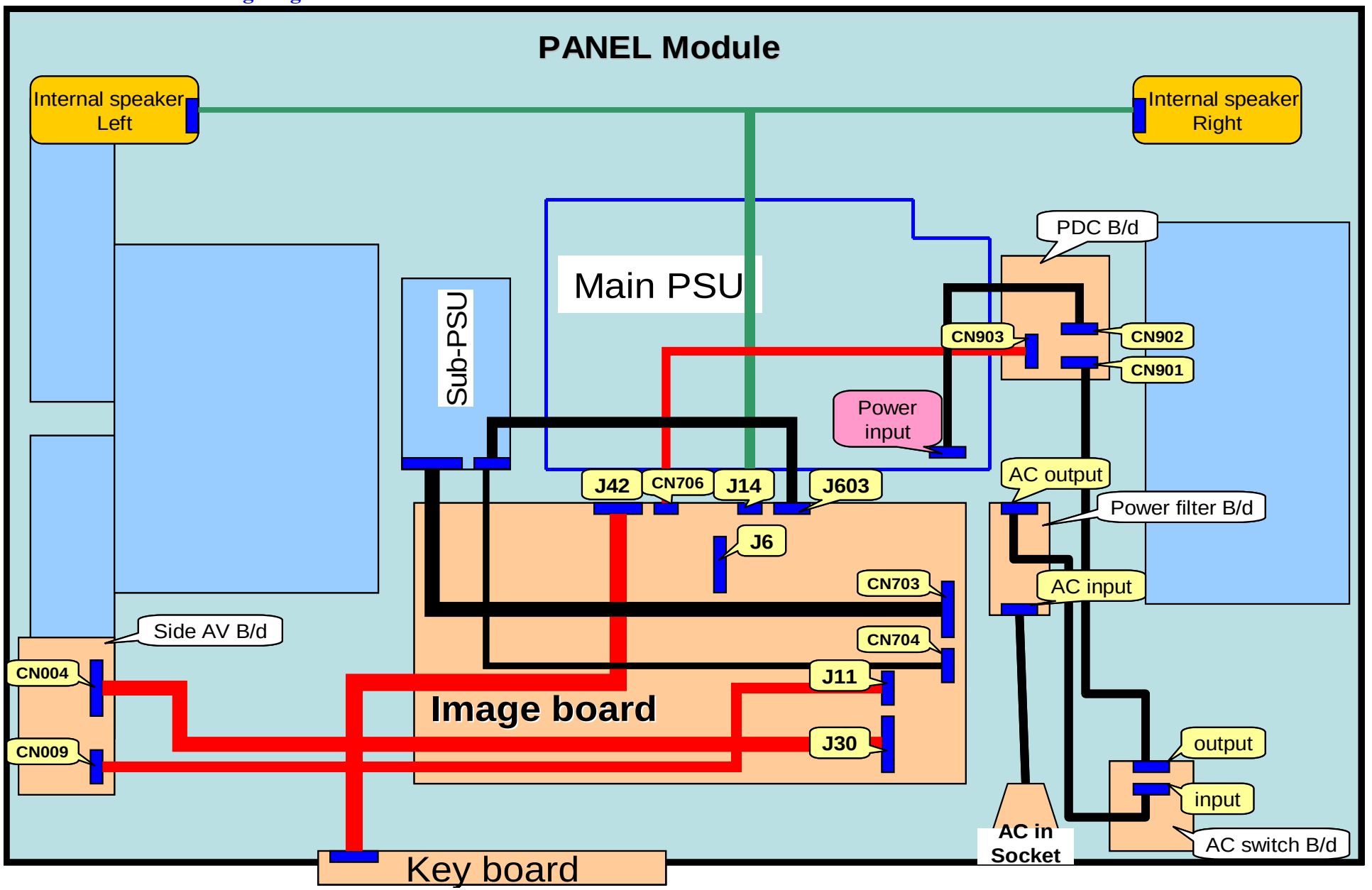


2) Remove all the aluminum foil around the panel (2), after assemble the new panel, must re-affix the aluminum foil, if it's broken must change a new one, otherwise, the EMI can be affected.
3) Remove the twelve silver screw around the PANEL corner (3).
4) Two people hold the panel holder 1 and 2 respectively, then uplift the panel module and move it out form the front cover(Bezel), and store in a safe place.



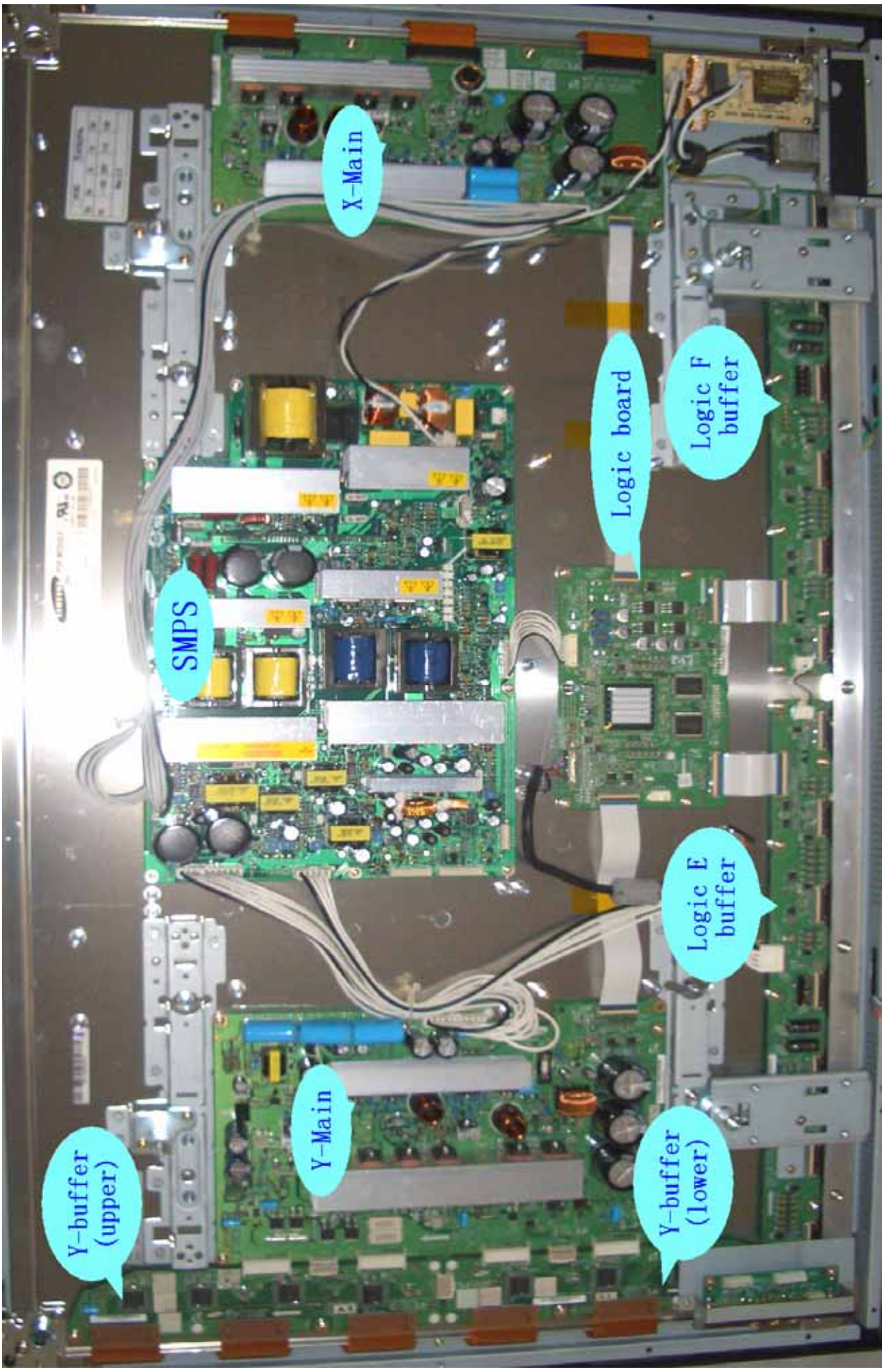
12-4 Block Wiring diagram

12-4-1 PDP boards block wiring diagram



No.	Pin Connection	Name	Pin function
1	J42 to Key board	MGPC key control signal output	**J42 Connector(13 Pins):** Pin 1= GND Pin 2= +5VSB Pin 3= IR Pin 4= ENTER Pin 5= LED-B Pin 6=LED-A Pin 7=KEY6 Pin 8=CH+ Pin 9= CH- Pin 10=VOL+ Pin 11=VOL- Pin 12=MENU Pin 13=TV video
2	CN706 to CN903	PDC board DC output, and MGPC standby PDC power control output	**CN706 Connector(4 Pins):** Pin 1,3= GND Pin 2=+5VSB Pin 4=REL-SW **CN903 Connector(4 Pins):** Pin 1,3= GND Pin 2=+5VSB Pin 4=PS-ON
3	J14 to speaker	MGPC audio signal output	**J14 Connector (2 Pins+2 Pins):** LO+/COMLO- and RO+/COMRO-
4	J603 to Sub-PSU	MGPC audio circuit power input	**J603 Connector(6 Pins):** Pin 1,2=+12V Audio Pin 3,4,6=GND Pin 5 = NC
5	CN703 to Sub-PSU	MGPC power input and relay control output	**CN703 Connector(11 Pins):** Pin 1=NC Pin 2=STB5V Pin 4=Relay-SW Pin 5=D12V Pin 8,9=D3.3V Pin 11=D6V Pin 3,6,7,10 =GND
6	CN704 to Sub-PSU	MGPC power input	**CN704 Connector(5 Pins):** Pin 1=D6V Pin 3=D12V Pin 2,4=GND Pin 5=NC
7	J11 to CN004	To Earphone output	**J11 Connector(5 Pins):** Pin 1,3=GND Pin 2=EAR-L Pin 4 = EAR-R Pin 5=Phone-on
8	J30 to CN009	Side AV signal input	J30 Connector(10 Pins): Pin 1,3,5,9=GND Pin 2=CVBS IN-2 Pin 4=FRONT-Y Pin 6=FRONT-C Pin 7=FRONT-AV-SEL Pin 8=SM-L Pin 10=SM-R
9	J6 to Panel Logic b/d	MGPC LVDS signal output	**J6 LVDS connector(31 Pins):** Pin 1,8,9=NC Pin 2,4,6,11,14,15,18,19, 22,23,26,27,30,31=GND Pin 12=TXE3p Pin 13=TXE3m Pin 16=TXECp Pin 17=TXECm Pin 20=TXE2p Pin 21=TXE2m Pin 24=TXE1p Pin 25=TXE1m Pin 28=TXE0p Pin 29=TXE0m

12-4-2 Panel Wiring diagram



13、Image board PCB LAYOUT

13-1 Image board PCB LAYOUT

13-2 Key board PCB LAYOUT

13-3 Side AV board PCB LAYOUT

13-4 PDC board PCB LAYOUT

Detail LAYOUT diagram please see the attached file “715P1511-G-4-17.pcb”.

715P1511-1C

14、Schematic diagram

Sheet Index

Page 01 - Title Sheet
Page 02 - Local Bus I/F
Page 03 - DDR SDRAM 0 I/F
Page 04 - Tuner / Demodulator
Page 05 - Video / Audio In
Page 06 - HDMI I/F
Page 07 - Analog Video Inputs
Page 08 - Decoder/Transport I/F
Page 09 - Video Prime / LVDS
Page 10 - Video Interface
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Page 12 - SIO / VCXO /Reset
Page 13 - Unused / GPIOs Block
Page 14 - Utility/JTAG Connectors
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Page 19 - Power and Gnd 5
Page 20 - GPIOs Table

Stuffing Options DTV Module

A) **R3 - OUT Power-On Auto-Read Operation DISABLED (for Samsung 256M ONLY). ***
R3 - OUT Power-On Auto-Read Operation ENABLED (for Samsung 256M ONLY).

B) **TP1-TP18 - IN -For R&D board only. ***
TP1-TP18 - OUT - For final board rev.

C) **R7- IN, R8 - OUT Normal boot-up from SPI.***
R7- OUT, R8 - IN Boot-up from NAND flash.

D) **R525, R528 - OUT ***
R525, R528 - IN - LCD Backlight levels setup.

E) **D49,R583,R585 - IN, R584, R586 - OUT -- Extornal Vref tor G9 DACs ***
D49,R583,R585 - OUT, R584, R586 - IN -- Intornal Vref tor G9 DACs *

F) **R342, R343 - IN, RS232 Utility card enable.**
R342, R343 - OUT, G-Link connector enable.

Note: * - Default setting.

Utility Board Jumper Options

1) J[22,23,24] = Boot DeviceSelection
   111 = boot from LB 8-bit data device with EXTERNAL PCI clock
   110 = boot from LB 16-bit data device with EXTERNAL PCI clock
   101 = boot from I2C 16-bit address 400 KHz device
   100 = boot from I2C 16-bit address 100 KHz device
   011 = boot from LB 8-bit data device with internal PCI clock (27 MHz)
   010 = boot from LB 16-bit data device with internal PCI clock (27 MHz)
   001 = boot from SPI 24-bit address/ 8-bit data device, 1 MHz clock
   000 = boot from SPI 16-bit address/ 8-bit data device, 1 MHz clock
2) J27 - OFF - EJTAG mode
   J27 - ON - JTAG mode
3) J16 - ON, J20 - 2-3 -- U23 Flash - CS0, U24 StrataFlash - CS1
   J16 - OFF, J20 - 1-2 -- U23 Flash - CS Disc., U24 StrataFlash - CS0
4) J17 - ON, - U24 StrataFlash memory contents cannot be altered.
5) J18 - OFF - StrataFlash device in x16 mode,
   J18 - ON- StrataFlash device in x8 mode.

Revision History

Revision	Description	P. Mgr.	Date
A	Initial Release		
D2	U9 IC setting and power bypass changes		
D2	R342, R343 , MSP34XX , TA2024 added WSD		

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Notes: (unless otherwise stated)

1. All resistors are listed in ohms and are 5%, 1/16W, Metal Film (0603 form factor)
2. All capacitors are listed in microfarads, and are 10%, 25V, ceramic, X7R (0603 form factor)
3. All inductors are listed in microhenries, and are 5%, 100ma, non-wound (0805 form factor)
4. "Signal Ports" and "Off Page Connectors" are Global, and transition between sheets.
5. Signal "Names" without "Signal Ports" or "Off Page Connectors" are Local, and only connect like named signals on the same sheet.

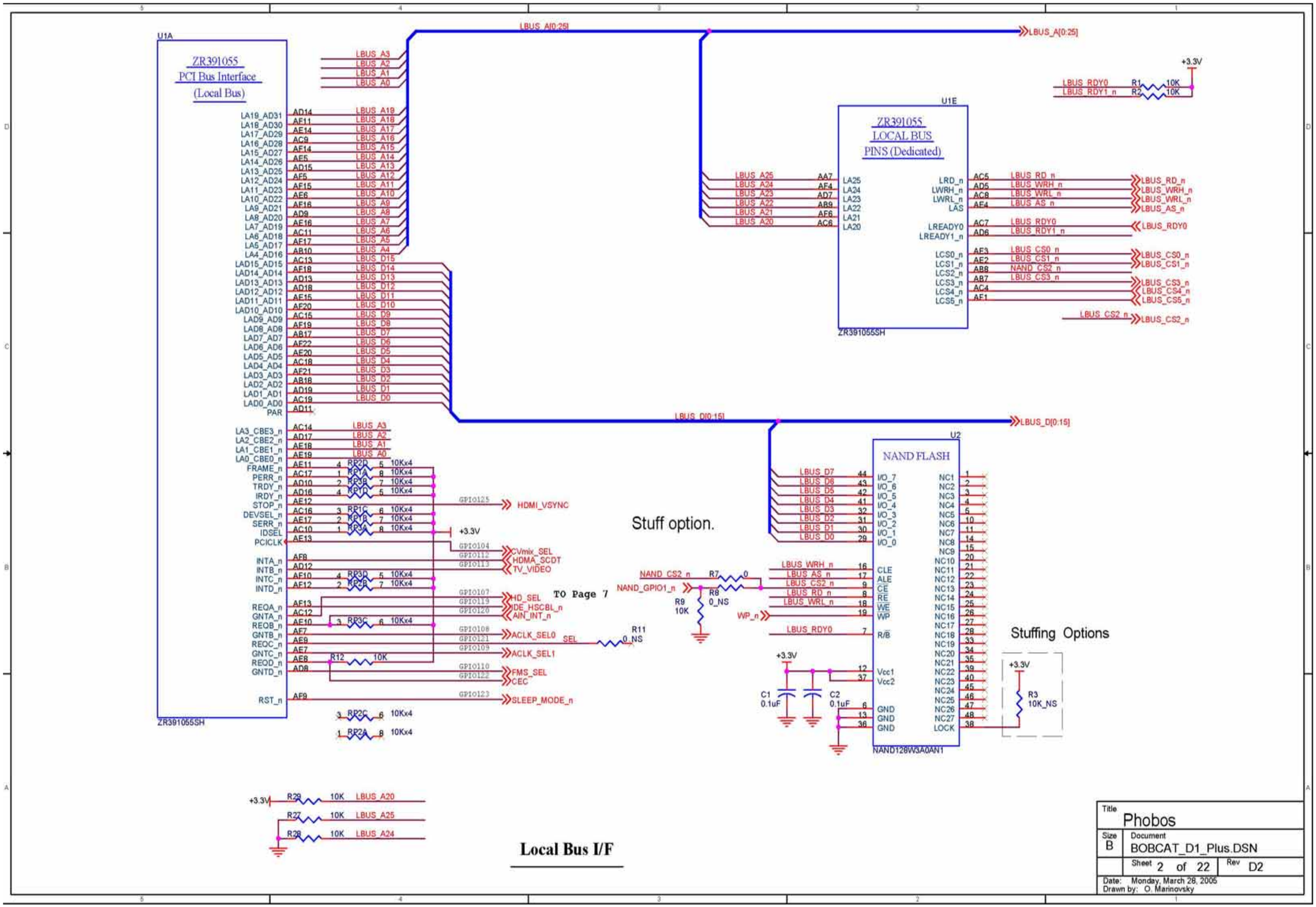
Project :
ATSC PDP TV

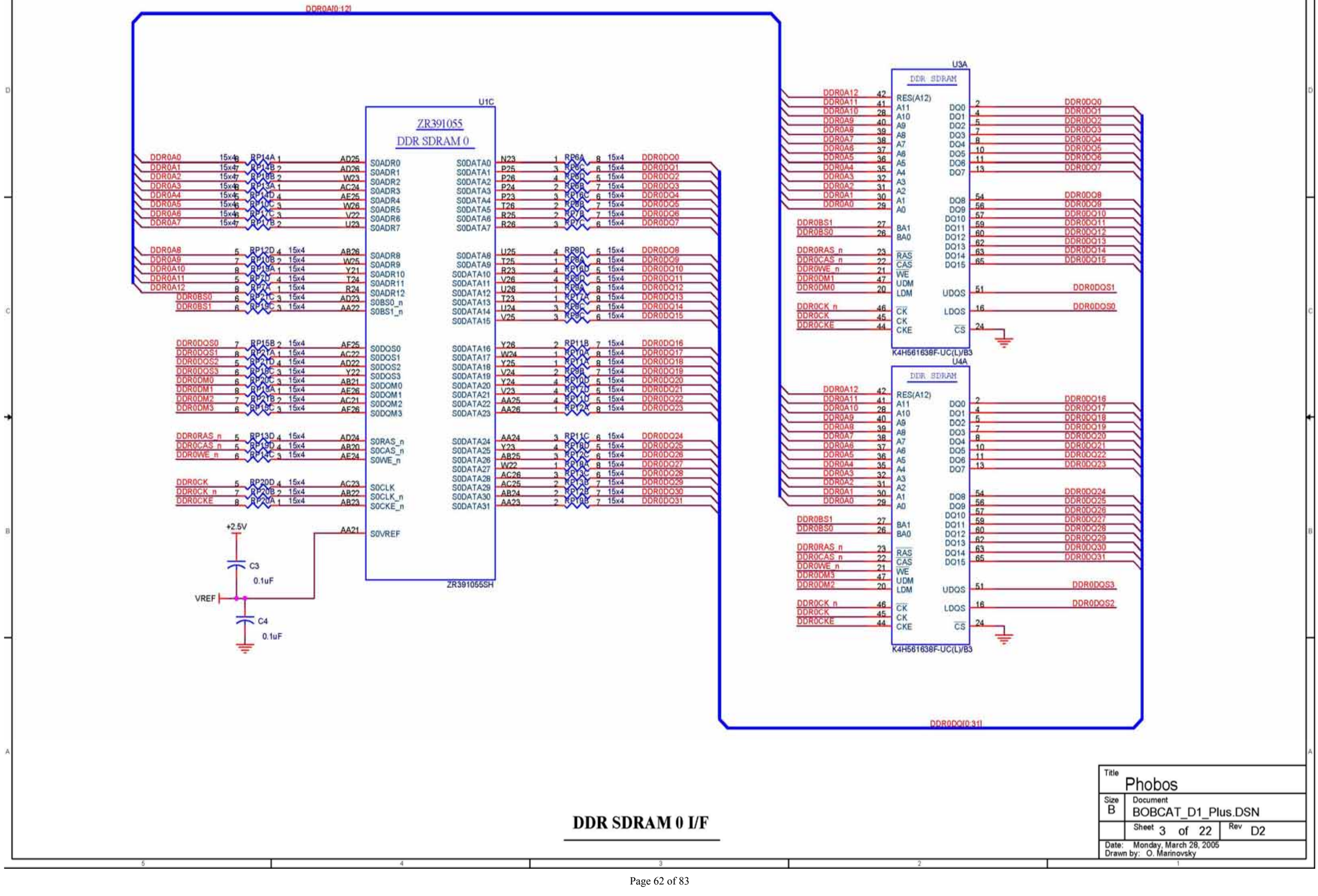
OTPV

PDP RD , NO.10 JiuXian Road
ChaoYang BeiJing , China
(0086) 010-64326699 EXT 8618

Reference:		Release Approvals
Fab:	<Fab #>	Applications
Assy:	<Assy #>	Marketing
Schem	N/A	Operations
Tree	<Tree #>	Product Mgr.

Title: Phobos D2
Size: B
Document: BOBCAT_D1_Plus.DSN
Sheet 1 of 22
Rev D2
Date: Monday, March 28, 2005
Drawn by: O. Marinovsky


U1A
ZR391055
PCI Bus Interface
(Local Bus)
ZR391055SH
LBUS_A[0:25]
LBUS_A[0:25]
LBUS_D[0:15]
LBUS_D[0:15]
U1E
ZR391055
LOCAL BUS
PINS (Dedicated)
ZR391055SH
+3.3V
LBUS_RDY0
LBUS_RDY1_n
R1 10K
R2 10K
U2
NAND FLASH
NAND128W3A0AN1
Stuff option.
Stuffing Options
TO Page 7
HDMI_VSYNC
CVmix_SEL
HDMA_SCDT
TV_VIDEO
HD_SEL
IDE_HSCBL_n
AIN_INT_n
ACLK_SEL0
ACLK_SEL1
FMS_SEL
CEC
SLEEP_MODE_n
Local Bus I/F
Title
Phobos
Size B
Document
BOBCAT_D1_Plus.DSN
Sheet 2 of 22
Rev D2
Date: Monday, March 28, 2005
Drawn by: O. Marinovsky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U1C
ZR391055
DDR SDRAM 0
ZR391055SH
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S0ADR1
S0ADR2
S0ADR3
S0ADR4
S0ADR5
S0ADR6
S0ADR7
S0ADR8
S0ADR9
S0ADR10
S0ADR11
S0ADR12
S0BS0_n
S0BS1_n
S0DQS0
S0DQS1
S0DQS2
S0DQS3
S0DQM0
S0DQM1
S0DQM2
S0DQM3
S0RAS_n
S0CAS_n
S0WE_n
S0CLK
S0CLK_n
S0CKE_n
S0VREF
S0DATA0
S0DATA1
S0DATA2
S0DATA3
S0DATA4
S0DATA5
S0DATA6
S0DATA7
S0DATA8
S0DATA9
S0DATA10
S0DATA11
S0DATA12
S0DATA13
S0DATA14
S0DATA15
S0DATA16
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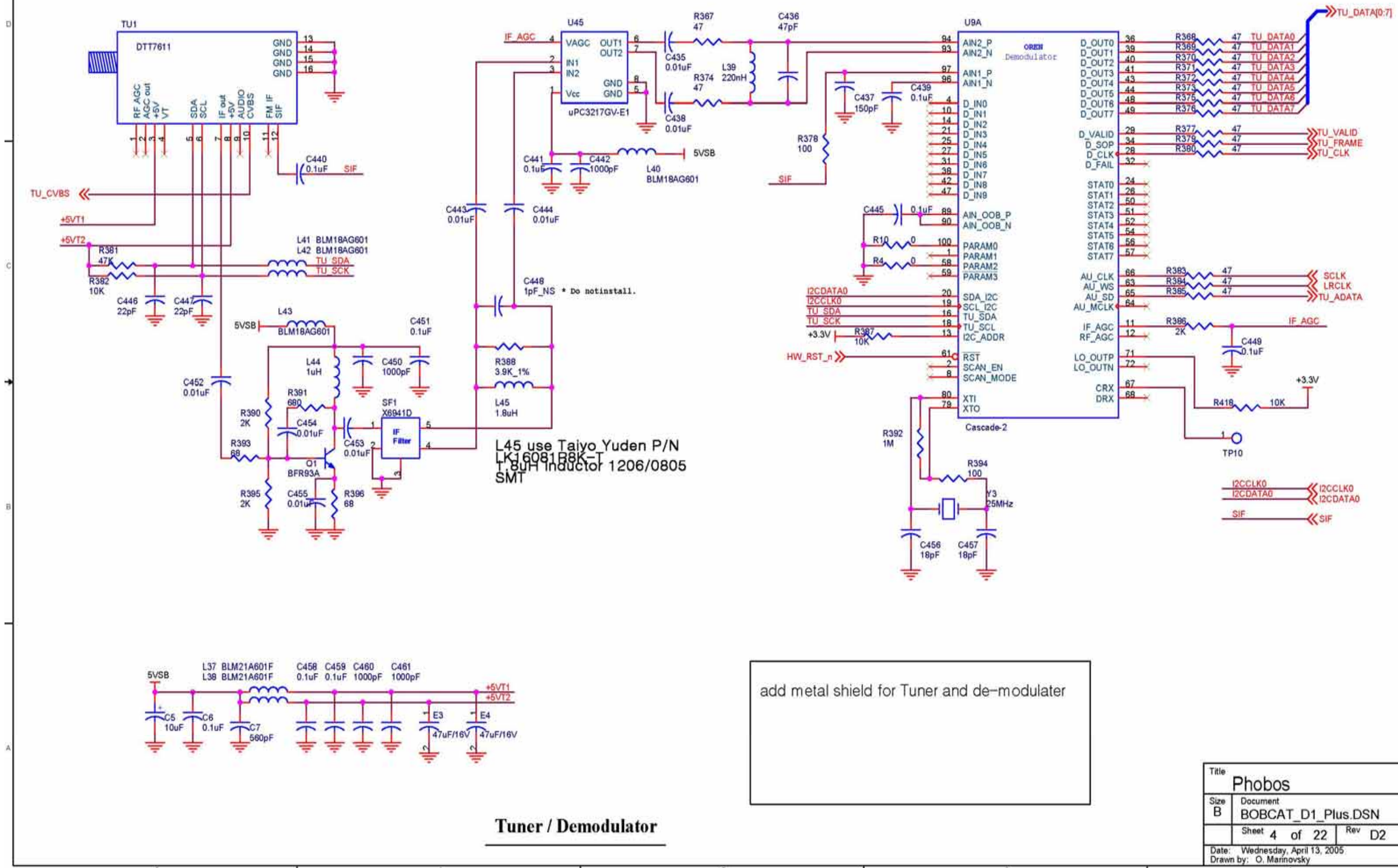
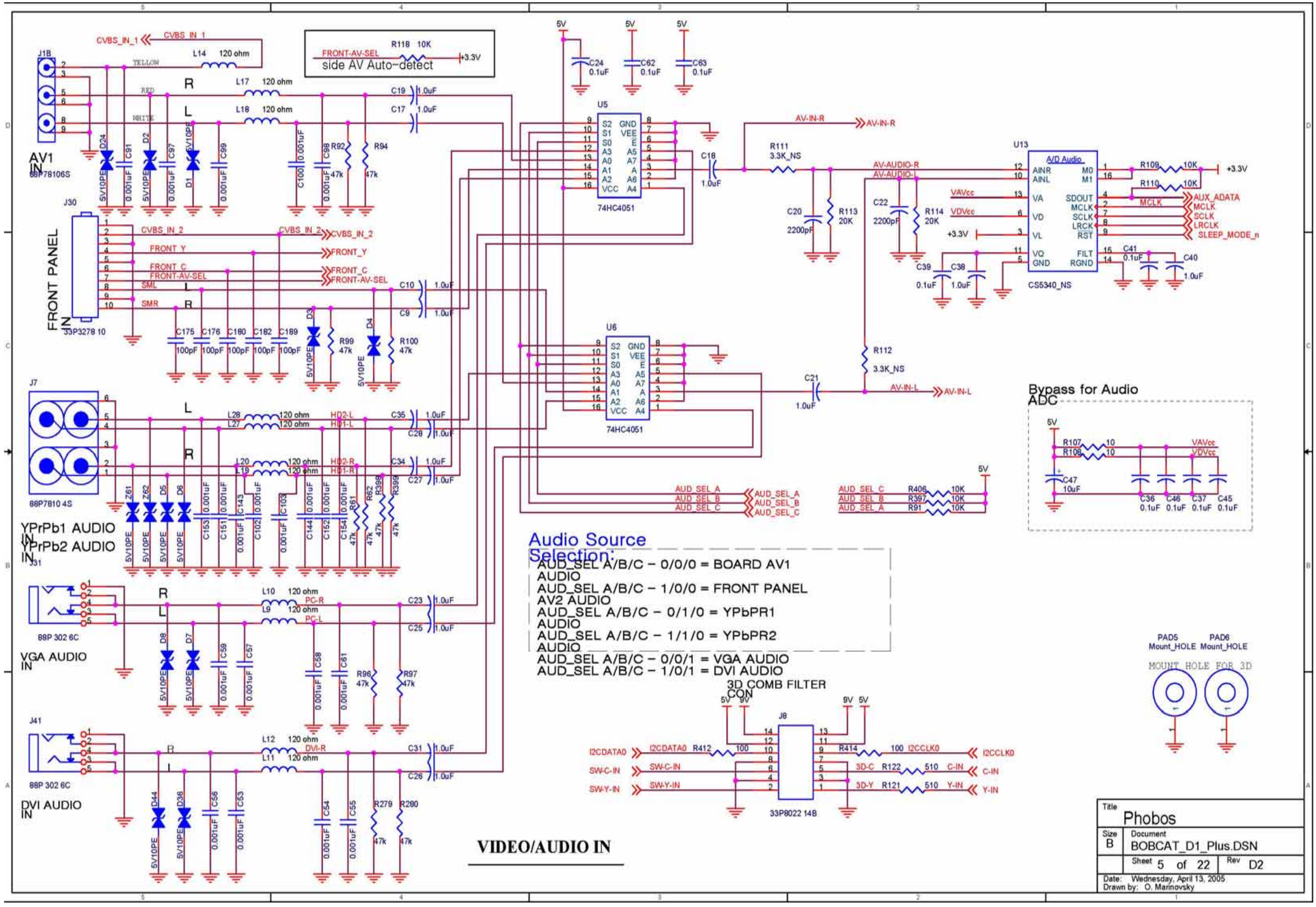
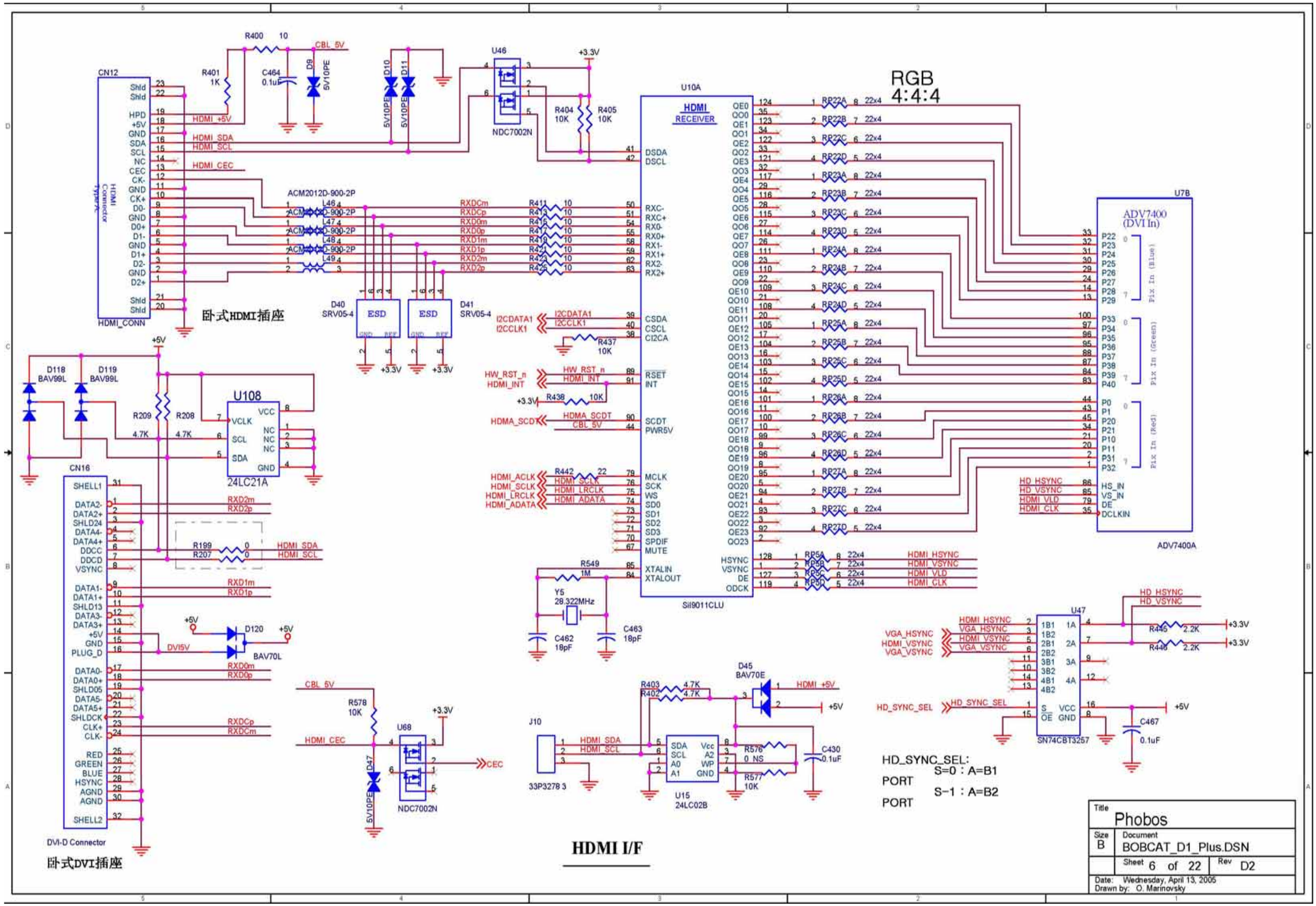
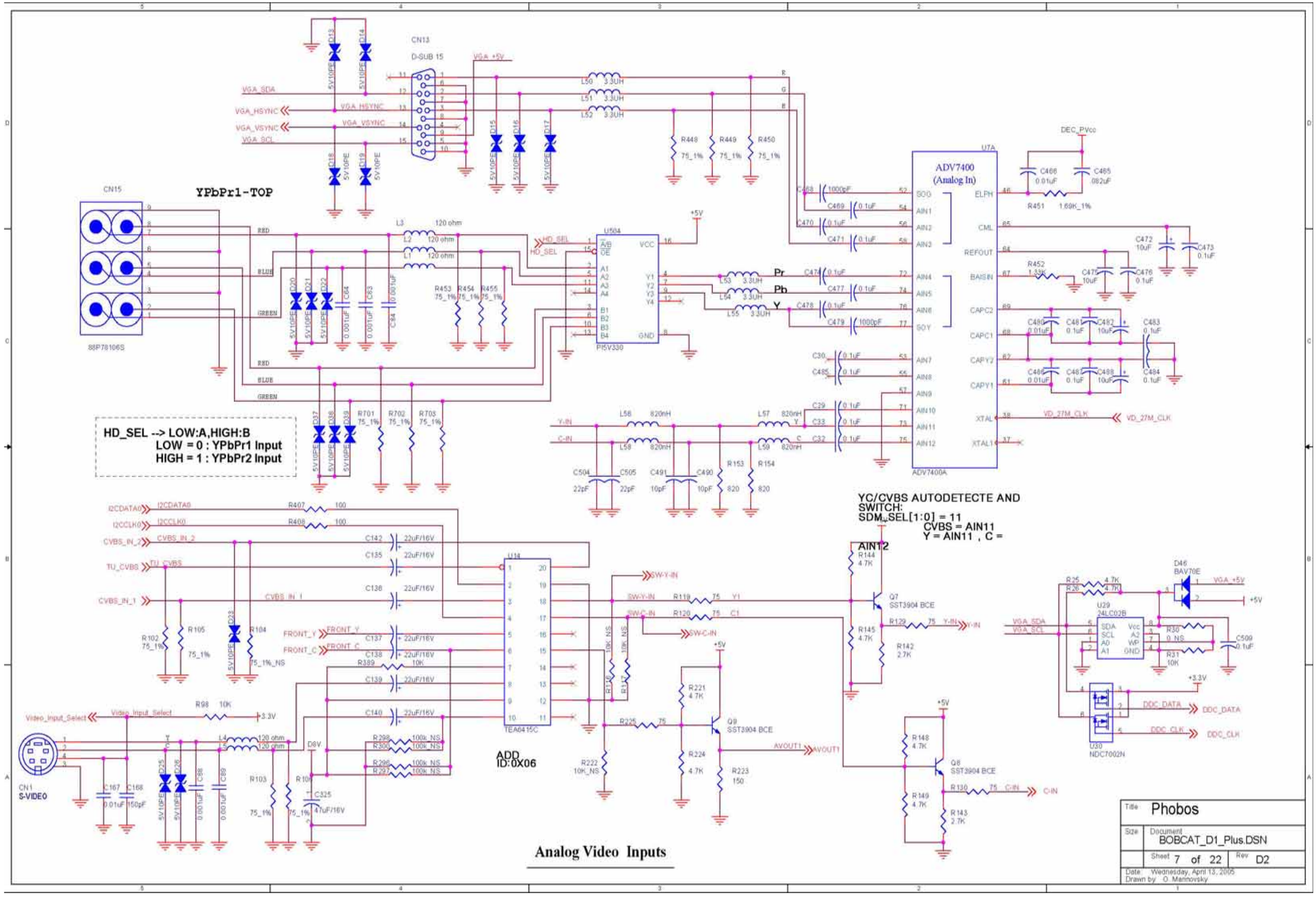
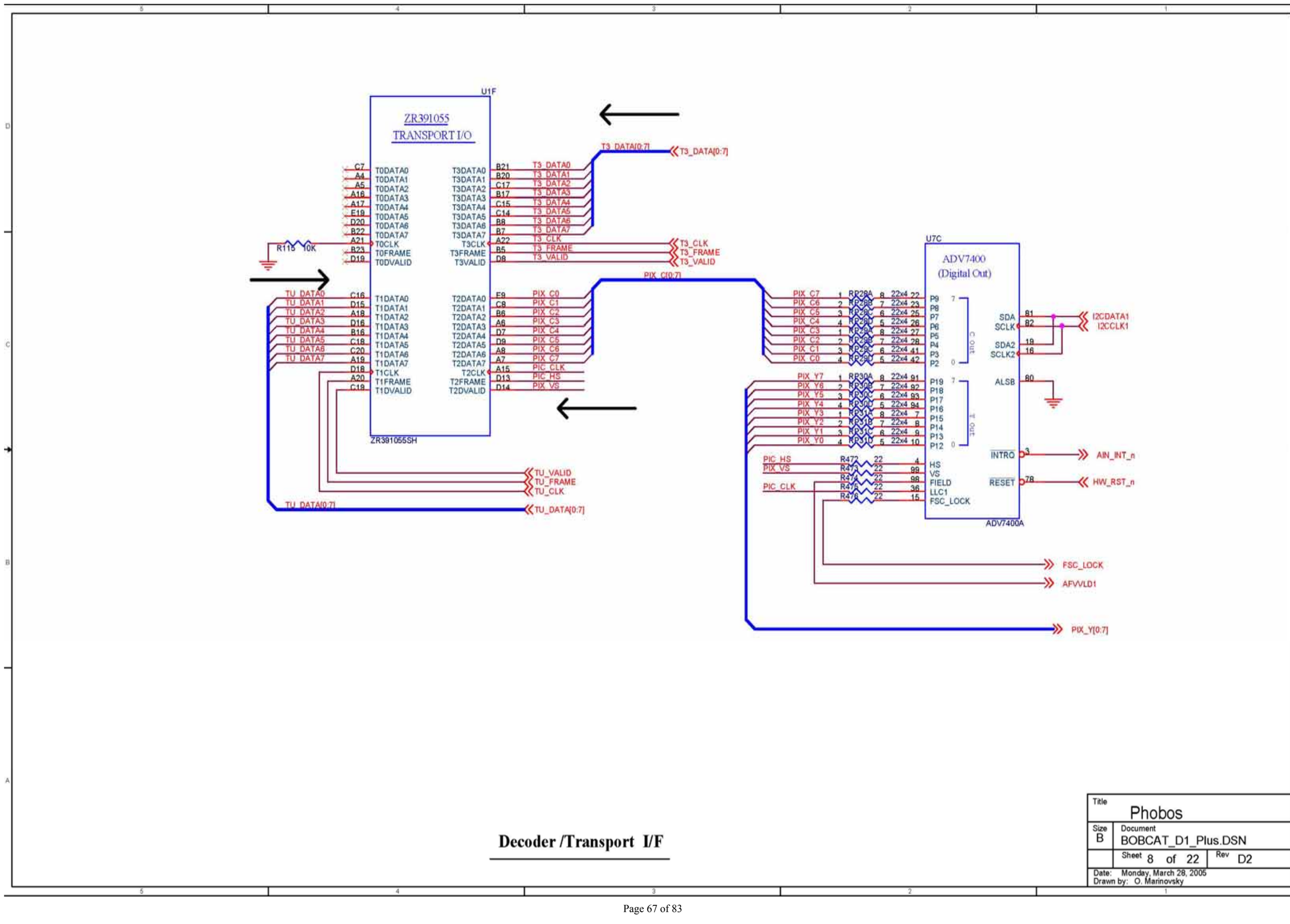
S0DATA20
S0DATA21
S0DATA22
S0DATA23
S0DATA24
S0DATA25
S0DATA26
S0DATA27
S0DATA28
S0DATA29
S0DATA30
S0DATA31
+2.5V
C3
0.1uF
VREF
C4
0.1uF
U3A
U4A
DDR SDRAM
K4H561638F-UC(L)/B3
DDR0DQ[0:31]
DDR0DQS0
DDR0DQS1
DDR0DQS2
DDR0DQS3
Title
Phobos
Size
B
Document
BOBCAT_D1_Plus.DSN
Sheet 3 of 22
Rev D2
Date: Monday, March 28, 2005
Drawn by: O. Marinovsky
DDR SDRAM 0 I/F

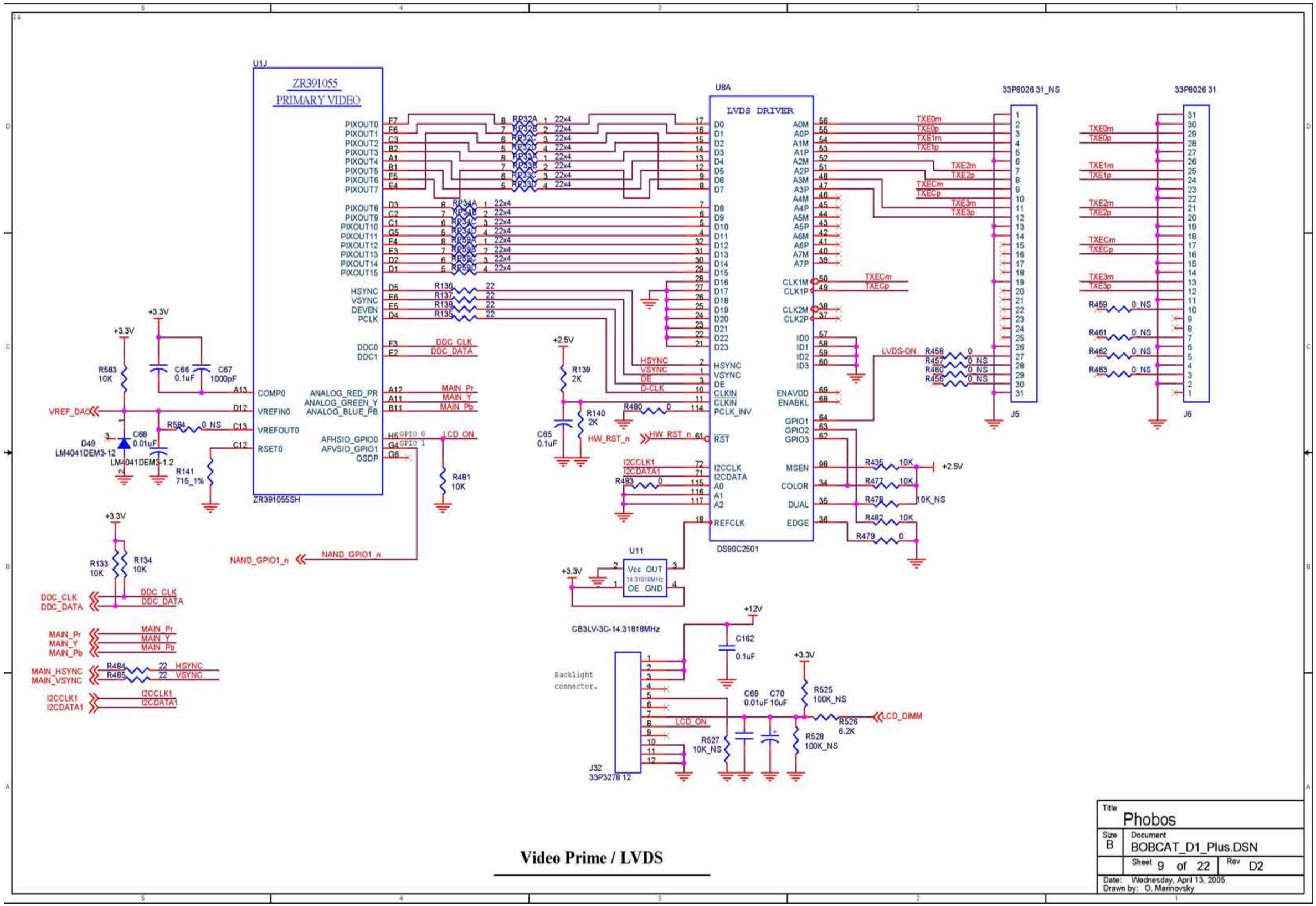

TU1
DTT7611
GND
GND
GND
GND
RF AGC
AGC out
+5V
VT
SDA
SCL
IF out
+5V
AUDIO
CVBS
FM IF
SIF
C440
0.1uF
SIF
TU_CVBS
+5VT1
+5VT2
R381
47K
R382
10K
C446
22pF
C447
22pF
L41 BLM18AG601
L42 BLM18AG601
TU_SDA
TU_SCK
5VSB
L43
BLM18AG601
C451
0.1uF
L44
1uH
C450
1000pF
C452
0.01uF
R391
680
R390
2K
C454
0.01uF
R393
68
Q1
BFR93A
C453
0.01uF
SF1
X6941D
IF
Filter
R395
2K
C455
0.01uF
R396
68
R388
3.9K_1%
L45
1.8uH
L45 use Taiyo Yuden P/N
LKJ6081R8K-T
1.8uH Inductor 1206/0805
SMT
U45
IF_AGC
VAGC
OUT1
OUT2
IN1
IN2
GND
GND
Vcc
uPC3217GV-E1
R367
47
C435
0.01uF
R374
47
C438
0.01uF
L39
220nH
C436
47pF
C441
0.1uF
C442
1000pF
5VSB
L40
BLM18AG601
C443
0.01uF
C444
0.01uF
C448
1pF_NS * Do notinstall.
R378
100
SIF
C437
150pF
C439
0.1uF
U9A
AIN2_P
AIN2_N
AIN1_P
AIN1_N
D_IN0
D_IN1
D_IN2
D_IN3
D_IN4
D_IN5
D_IN6
D_IN7
D_IN8
D_IN9
ORION
Demodulator
C445
0.1uF
AIN_OOB_P
AIN_OOB_N
R10
0
R4
0
PARAM0
PARAM1
PARAM2
PARAM3
I2CDATA0
I2CCLK0
TU_SDA
TU_SCK
SDA_I2C
SCL_I2C
TU_SDA
TU_SCL
I2C_ADDR
+3.3V
R387
10K
HW_RST_n
RST
SCAN_EN
SCAN_MODE
XTI
XTO
Cascade-2
R392
1M
R394
100
Y3
25MHz
C456
18pF
C457
18pF
D_OUT0
D_OUT1
D_OUT2
D_OUT3
D_OUT4
D_OUT5
D_OUT6
D_OUT7
TU_DATA[0:7]
R368
R369
R370
R371
R372
R373
R375
R376
TU_DATA0
TU_DATA1
TU_DATA2
TU_DATA3
TU_DATA4
TU_DATA5
TU_DATA6
TU_DATA7
D_VALID
D_SOP
D_CLK
D_FAIL
R377
R379
R380
TU_VALID
TU_FRAME
TU_CLK
STAT0
STAT1
STAT2
STAT3
STAT4
STAT5
STAT6
STAT7
AU_CLK
AU_WS
AU_SD
AU_MCLK
R383
R384
R385
SCLK
LRCLK
TU_ADATA
IF_AGC
RF_AGC
R386
2K
C449
0.1uF
LO_OUTP
LO_OUTN
CRX
DRX
R418
10K
+3.3V
TP10
I2CCLK0
I2CDATA0
SIF
L37 BLM21A601F
L38 BLM21A601F
C458
0.1uF
C459
0.1uF
C460
1000pF
C461
1000pF
C5
10uF
C6
0.1uF
C7
560pF
E3
47uF/16V
E4
47uF/16V
add metal shield for Tuner and de-modulater
Tuner / Demodulator
Title
Phobos
Size
B
Document
BOBCAT_D1_Plus.DSN
Sheet 4 of 22
Rev D2
Date: Wednesday, April 13, 2005
Drawn by: O. Marinovsky

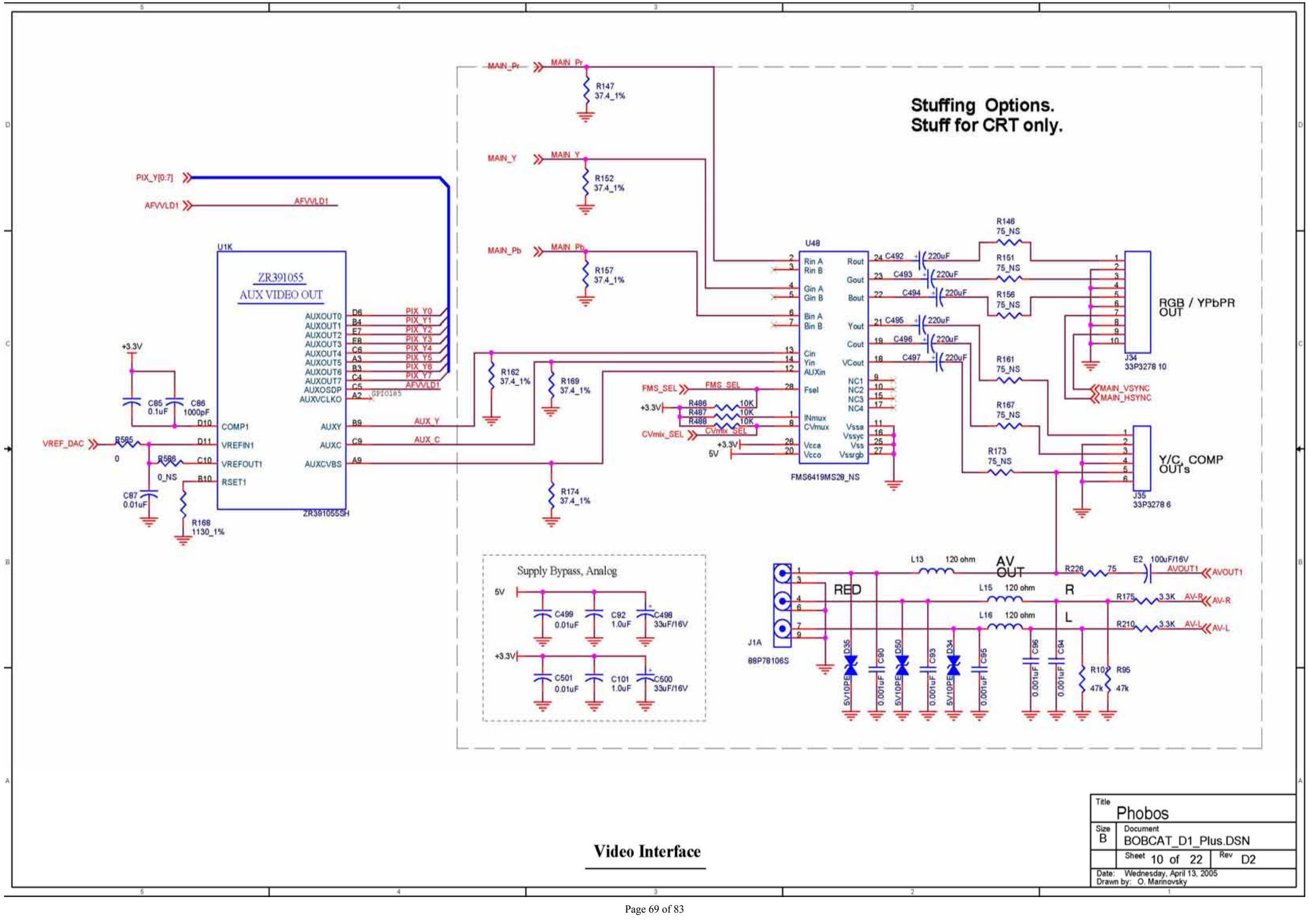

FRONT-AV-SEL
R118 10K
+3.3V
side AV Auto-detect
AV1 IN
88P78106S
FRONT PANEL IN
33P3278 10
74HC4051
A/D Audio
CS5340_NS
Bypass for Audio ADC
AUDIO SOURCE SELECTION:
AUD_SEL A/B/C – 0/0/0 = BOARD AV1 AUDIO
AUD_SEL A/B/C – 1/0/0 = FRONT PANEL AV2 AUDIO
AUD_SEL A/B/C – 0/1/0 = YPbPR1 AUDIO
AUD_SEL A/B/C – 1/1/0 = YPbPR2 AUDIO
AUD_SEL A/B/C – 0/0/1 = VGA AUDIO
AUD_SEL A/B/C – 1/0/1 = DVI AUDIO
3D COMB FILTER CON
33P8022 14B
YPrPb1 AUDIO IN
YPrPb2 AUDIO IN
88P7810 4S
VGA AUDIO IN
88P 302 6C
DVI AUDIO IN
88P 302 6C
VIDEO/AUDIO IN
PAD5 Mount_HOLE
PAD6 Mount_HOLE
MOUNT HOLE FOR 3D
Title Phobos
Size B
Document BOBCAT_D1_Plus.DSN
Sheet 5 of 22
Rev D2
Date: Wednesday, April 13, 2005
Drawn by: O. Marinovsky

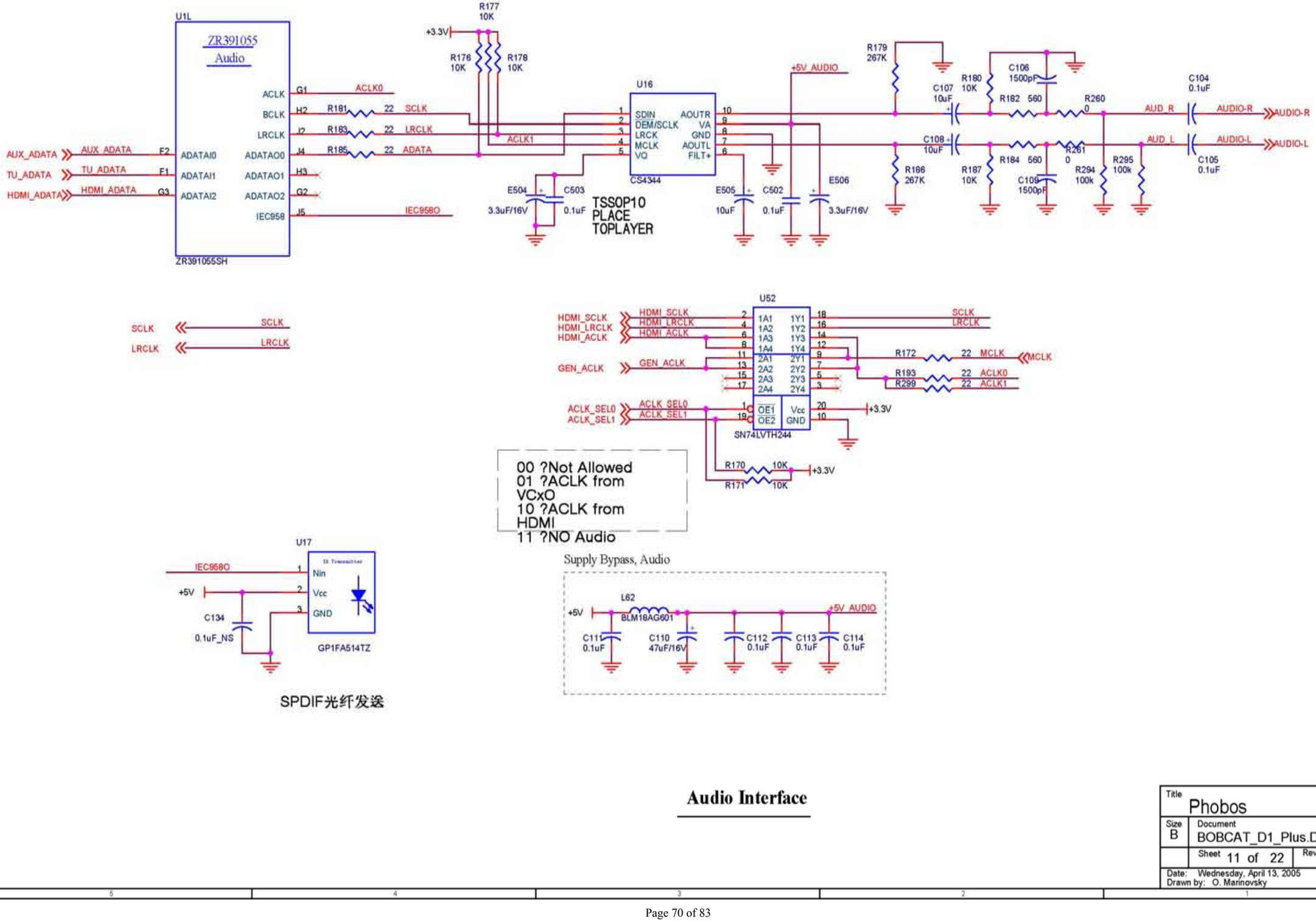

RGB
4:4:4
HDMI I/F
卧式HDMI插座
卧式DVI插座
DVI-D Connector
HDMI_CONN
CN12
CN16
U10A
HDMI
RECEIVER
Sil9011CLU
U7B
ADV7400
(DVI In)
ADV7400A
U108
24LC21A
U68
NDC7002N
U46
NDC7002N
U47
SN74CBT3257
U15
24LC02B
J10
33P3278 3
D40
SRV05-4
D41
SRV05-4
ESD
D118
BAV99L
D119
BAV99L
D120
BAV70L
D45
BAV70E
D9
5V10PE
D10
5V10PE
D11
5V10PE
D47
5V10PE
ACM2012D-900-2P
L46,4
L47,4
L48,4
L49,4
R400 10
R401 1K
C464 0.1uF
R404 10K
R405 10K
R411 10
R412 10
R415 10
R416 10
R419 10
R420 10
R423 10
R424 10
R437 10K
R438 10K
R442 22
R549 1M
R199 0
R207 0
R209 4.7K
R208 4.7K
R578 10K
R403 4.7K
R402 4.7K
R576 0 NS
R577 10K
C462 18pF
C463 18pF
C430 0.1uF
C467 0.1uF
R445 2.2K
R446 2.2K
Y5
28.322MHz
CBL_5V
HDMI_+5V
HDMI_SDA
HDMI_SCL
HDMI_CEC
RXDCm
RXDCp
RXD0m
RXD0p
RXD1m
RXD1p
RXD2m
RXD2p
I2CDATA1
I2CCLK1
HW_RST_n
HDMI_INT
HDMA_SCDT
HDMI_ACLK
HDMI_SCLK
HDMI_LRCLK
HDMI_ADATA
HDMI_HSYNC
HDMI_VSYNC
HDMI_VLD
HDMI_CLK
HD_HSYNC
HD_VSYNC
VGA_HSYNC
VGA_VSYNC
HD_SYNC_SEL
DVI5V
+5V
+3.3V
CEC
HD_SYNC_SEL:
S=0 : A=B1
PORT
S-1 : A=B2
PORT
Title
Phobos
Size
B
Document
BOBCAT_D1_Plus.DSN
Sheet 6 of 22
Rev D2
Date: Wednesday, April 13, 2005
Drawn by: O. Marinovsky

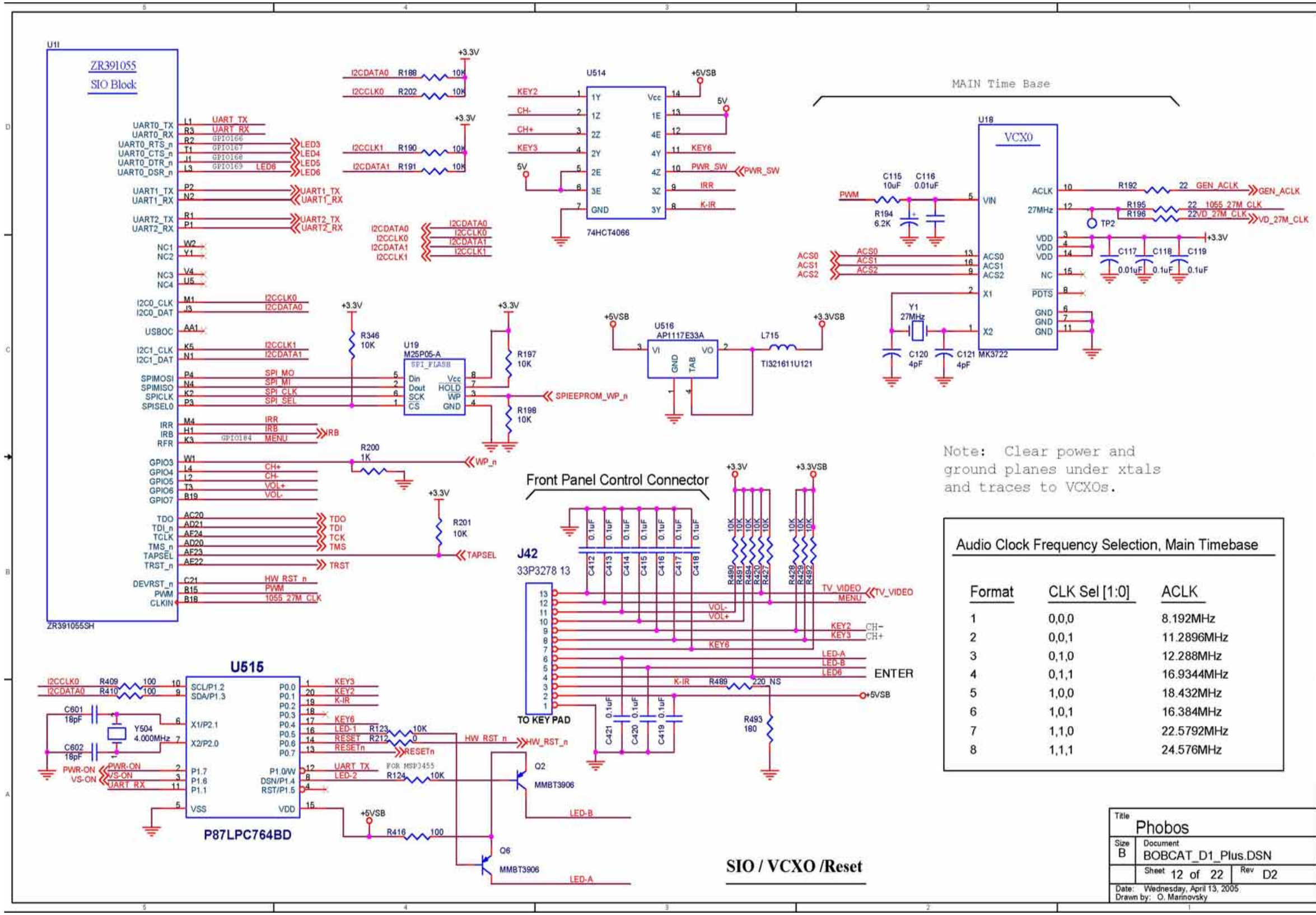

CN13
D-SUB 15
VGA_SDA
VGA_HSYNC
VGA_VSYNC
VGA_SCL
VGA +5V
CN15
YPbPr1-TOP
88P78106S
RED
BLUE
GREEN
L3 120 ohm
L2 120 ohm
L1 120 ohm
U504
PI5V330
HD_SEL
+5V
L50 3.3UH
L51 3.3UH
L52 3.3UH
R448 75_1%
R449 75_1%
R450 75_1%
R453 75_1%
R454 75_1%
R455 75_1%
L53 3.3UH
L54 3.3UH
L55 3.3UH
Pr
Pb
Y
U17A
ADV7400
(Analog In)
ADV7400A
DEC_PVcc
C466 0.01uF
C465 082uF
R451 1.69K_1%
C472 10uF
C473 0.1uF
R452 1.33K
C475 10uF
C476 0.1uF
C480 0.01uF
C481 0.1uF
C482 10uF
C483 0.1uF
C486 0.01uF
C487 0.1uF
C488 10uF
C484 0.1uF
VD_27M_CLK
HD_SEL --> LOW:A,HIGH:B
LOW = 0 : YPbPr1 Input
HIGH = 1 : YPbPr2 Input
Y-IN
C-IN
L56 820nH
L58 820nH
L57 820nH
L59 820nH
C504 22pF
C505 22pF
C491 10pF
C490 10pF
R153 820
R154 820
I2CDATA0
I2CCLK0
CVBS_IN_2
TU_CVBS
CVBS_IN_1
FRONT_Y
FRONT_C
R407 100
R408 100
C142 22uF/16V
C135 22uF/16V
C136 22uF/16V
C137 22uF/16V
C138 22uF/16V
C139 22uF/16V
C140 22uF/16V
R389 10K
R102 75_1%
R105 75_1%
R104 75_1%_NS
U14
TEA6415C
ADD
ID:0X06
SW-Y-IN
SW-C-IN
R119 75 Y1
R120 75 C1
R136 10K_NS
R137 10K_NS
R222 10K_NS
R225 75
R221 4.7K
R224 4.7K
Q9
SST3904 BCE
R223 150
AVOUT1
YC/CVBS AUTODETECTE AND
SWITCH:
SDM_SEL[1:0] = 11
CVBS = AIN11
Y = AIN11 , C =
AIN12
R144 4.7K
R145 4.7K
R142 2.7K
Q7
SST3904 BCE
R129 75 Y-IN
Y-IN
R148 4.7K
R149 4.7K
R143 2.7K
Q8
SST3904 BCE
R130 75 C-IN
C-IN
D46
BAV70E
VGA +5V
+5V
U29
24LC02B
R25 4.7K
R26 4.7K
R30 0_NS
R31 10K
C509 0.1uF
+3.3V
DDC_DATA
DDC_CLK
U30
NDC7002N
R98 10K
Video_Input_Select
CN1
S-VIDEO
C167 0.01uF
C168 150pF
L4 120 ohm
L5 120 ohm
D6V
R103 75_1%
R104 75_1%
C325 47uF/16V
R298 100k_NS
R300 100k_NS
R296 100k_NS
R297 100k_NS
Analog Video Inputs
Title Phobos
Size
Document BOBCAT_D1_Plus.DSN
Sheet 7 of 22
Rev D2
Date Wednesday, April 13, 2005
Drawn by O. Marinovsky


U1F
ZR391055
TRANSPORT I/O
ZR391055SH
T3_DATA[0:7]
T3_CLK
T3_FRAME
T3_VALID
R115 10K
PIX_C[0:7]
TU_VALID
TU_FRAME
TU_CLK
TU_DATA[0:7]
U7C
ADV7400
(Digital Out)
ADV7400A
SDA
SCLK
SDA2
SCLK2
I2CDATA1
I2CCLK1
ALSB
INTRO
AIN_INT_n
RESET
HW_RST_n
HS
VS
FIELD
LLC1
FSC_LOCK
PIC_HS
PIX_VS
PIC_CLK
FSC_LOCK
AFVVLD1
PIX_Y[0:7]
Decoder /Transport I/F
Title
Phobos
Size
B
Document
BOBCAT_D1_Plus.DSN
Sheet 8 of 22
Rev D2
Date: Monday, March 28, 2005
Drawn by: O. Marinovsky


U1J
ZR391055
PRIMARY VIDEO
PIXOUT0
PIXOUT1
PIXOUT2
PIXOUT3
PIXOUT4
PIXOUT5
PIXOUT6
PIXOUT7
PIXOUT8
PIXOUT9
PIXOUT10
PIXOUT11
PIXOUT12
PIXOUT13
PIXOUT14
PIXOUT15
HSYNC
VSYNC
DEVEN
PCLK
DDC0
DDC1
COMP0
VREFIN0
VREFOUT0
RSET0
ANALOG_RED_PR
ANALOG_GREEN_Y
ANALOG_BLUE_PB
AFHSIO_GPIO0
AFVSIO_GPIO1
OSDP
ZR391055SH
U8A
LVDS DRIVER
DS90C2501
33P8026 31_NS
33P8026 31
J5
J6
J32
33P3278 12
U11
CB3LV-3C-14.31818MHz
Backlight
connector.
LVDS-ON
LCD_ON
LCD_DIMM
HW_RST_n
NAND_GPIO1_n
MAIN_Pr
MAIN_Y
MAIN_Pb
MAIN_HSYNC
MAIN_VSYNC
I2CCLK1
I2CDATA1
DDC_CLK
DDC_DATA
TXE0m
TXE0p
TXE1m
TXE1p
TXE2m
TXE2p
TXECm
TXECp
TXE3m
TXE3p
+3.3V
+2.5V
+12V
Video Prime / LVDS
Title
Phobos
Size
B
Document
BOBCAT_D1_Plus.DSN
Sheet 9 of 22
Rev D2
Date: Wednesday, April 13, 2005
Drawn by: O. Marinovsky


Stuffing Options.
Stuff for CRT only.
ZR391055
AUX VIDEO OUT
U1K
ZR391055SH
PIX_Y[0:7]
AFVVLD1
MAIN_Pr
MAIN_Y
MAIN_Pb
R147 37.4_1%
R152 37.4_1%
R157 37.4_1%
R162 37.4_1%
R169 37.4_1%
R174 37.4_1%
R168 1130_1%
C85 0.1uF
C86 1000pF
C87 0.01uF
VREF_DAC
R585 0
R586 0_NS
COMP1
VREFIN1
VREFOUT1
RSET1
AUXY
AUXC
AUXCVBS
AUX_Y
AUX_C
U48
FMS6419MS28_NS
FMS_SEL
CVmix_SEL
R486 10K
R487 10K
R488 10K
RGB / YPbPR OUT
J34 33P3278 10
MAIN_VSYNC
MAIN_HSYNC
Y/C, COMP OUTs
J35 33P3278 6
R146 75_NS
R151 75_NS
R156 75_NS
R161 75_NS
R167 75_NS
R173 75_NS
C492 220uF
C493 220uF
C494 220uF
C495 220uF
C496 220uF
C497 220uF
Supply Bypass, Analog
C499 0.01uF
C92 1.0uF
C498 33uF/16V
C501 0.01uF
C101 1.0uF
C500 33uF/16V
L13 120 ohm
L15 120 ohm
L16 120 ohm
AV OUT
RED
R
L
R226 75
E2 100uF/16V
AVOUT1
R175 3.3K
AV-R
R210 3.3K
AV-L
J1A
88P78106S
D35
D50
D34
5V10PE
R102 47k
R95 47k
Video Interface
Title Phobos
Size B
Document BOBCAT_D1_Plus.DSN
Sheet 10 of 22
Rev D2
Date: Wednesday, April 13, 2005
Drawn by: O. Marinovsky

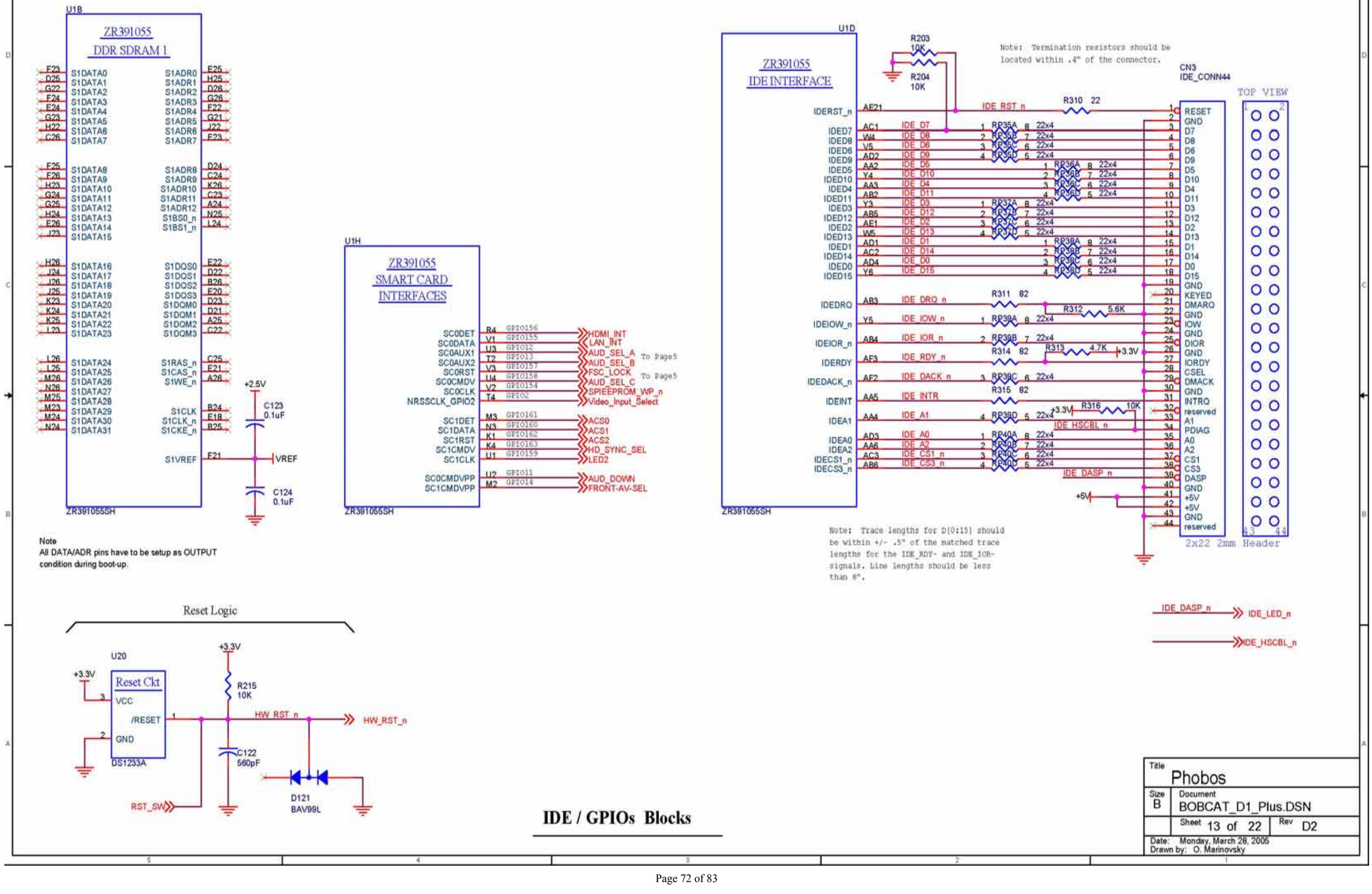

U1L
ZR391055
Audio
ACLK
BCLK
LRCLK
ADATAO0
ADATAO1
ADATAO2
IEC958
ADATAI0
ADATAI1
ADATAI2
ZR391055SH
AUX_ADATA
TU_ADATA
HDMI_ADATA
ACLK0
SCLK
LRCLK
ADATA
IEC958O
ACLK1
R177 10K
R176 10K
R178 10K
+3.3V
U16
SDIN
DEM/SCLK
LRCK
MCLK
VQ
AOUTR
GND
AOUTL
FILT+
VA
CS4344
TSSOP10
PLACE
TOPLAYER
+5V_AUDIO
R179 267K
R180 10K
C106 1500pF
C107 10uF
R182 560
R260 0
C104 0.1uF
AUD_R
AUDIO-R
C108 10uF
R184 560
R261 0
AUD_L
AUDIO-L
C105 0.1uF
R186 267K
R187 10K
C109 1500pF
R294 100k
R295 100k
E504 3.3uF/16V
C503 0.1uF
E505 10uF
C502 0.1uF
E506 3.3uF/16V
SCLK
LRCLK
U52
HDMI_SCLK
HDMI_LRCLK
HDMI_ACLK
GEN_ACLK
ACLK_SEL0
ACLK_SEL1
1A1 1A2 1A3 1A4
2A1 2A2 2A3 2A4
1Y1 1Y2 1Y3 1Y4
2Y1 2Y2 2Y3 2Y4
OE1 OE2
Vcc GND
SN74LVTH244
R172 22 MCLK
R193 22 ACLK0
R299 22 ACLK1
MCLK
R170 10K
R171 10K
00 ?Not Allowed
01 ?ACLK from VCxO
10 ?ACLK from HDMI
11 ?NO Audio
U17
IEC958O
+5V
Nin
Vcc
GND
C134 0.1uF_NS
GP1FA514TZ
SPDIF光纤发送
Supply Bypass, Audio
L62
BLM18AG601
C111 0.1uF
C110 47uF/16V
C112 0.1uF
C113 0.1uF
C114 0.1uF
Audio Interface
Title
Phobos
Size B
Document
BOBCAT_D1_Plus.DSN
Sheet 11 of 22
Rev D2
Date: Wednesday, April 13, 2005
Drawn by: O. Marinovsky

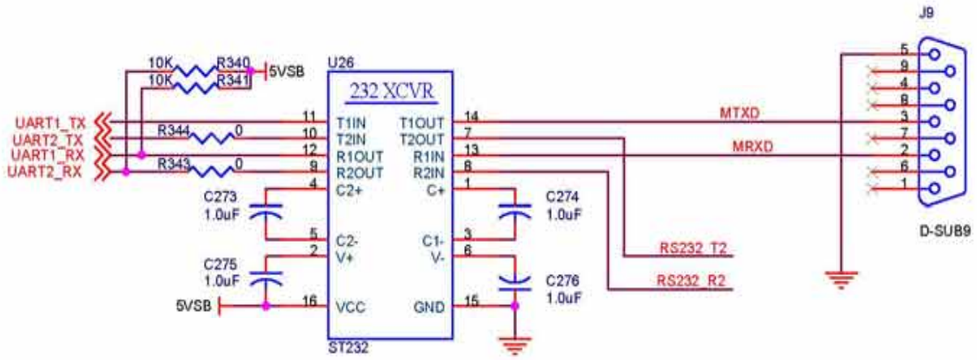


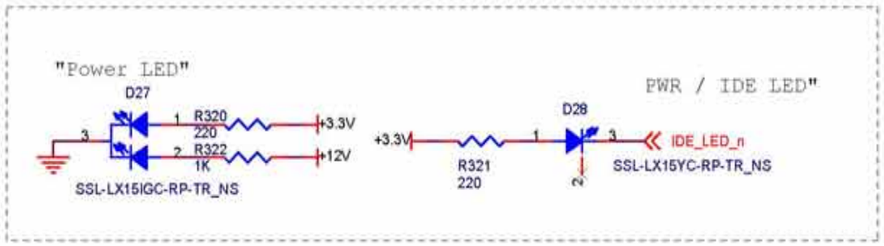
Audio Clock Frequency Selection, Main Timebase

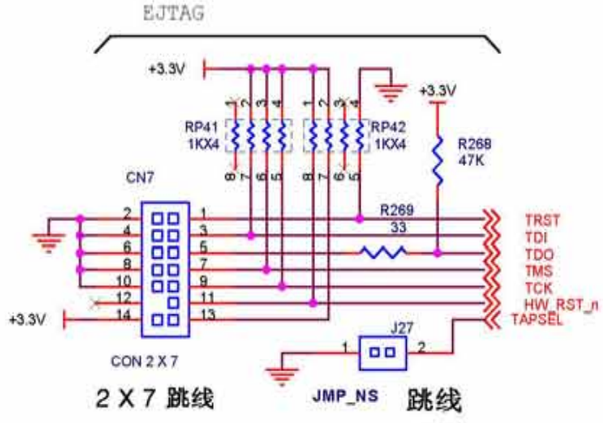
Format	CLK Sel [1:0]	ACLK
1	0,0,0	8.192MHz
2	0,0,1	11.2896MHz
3	0,1,0	12.288MHz
4	0,1,1	16.9344MHz
5	1,0,0	18.432MHz
6	1,0,1	16.384MHz
7	1,1,0	22.5792MHz
8	1,1,1	24.576MHz

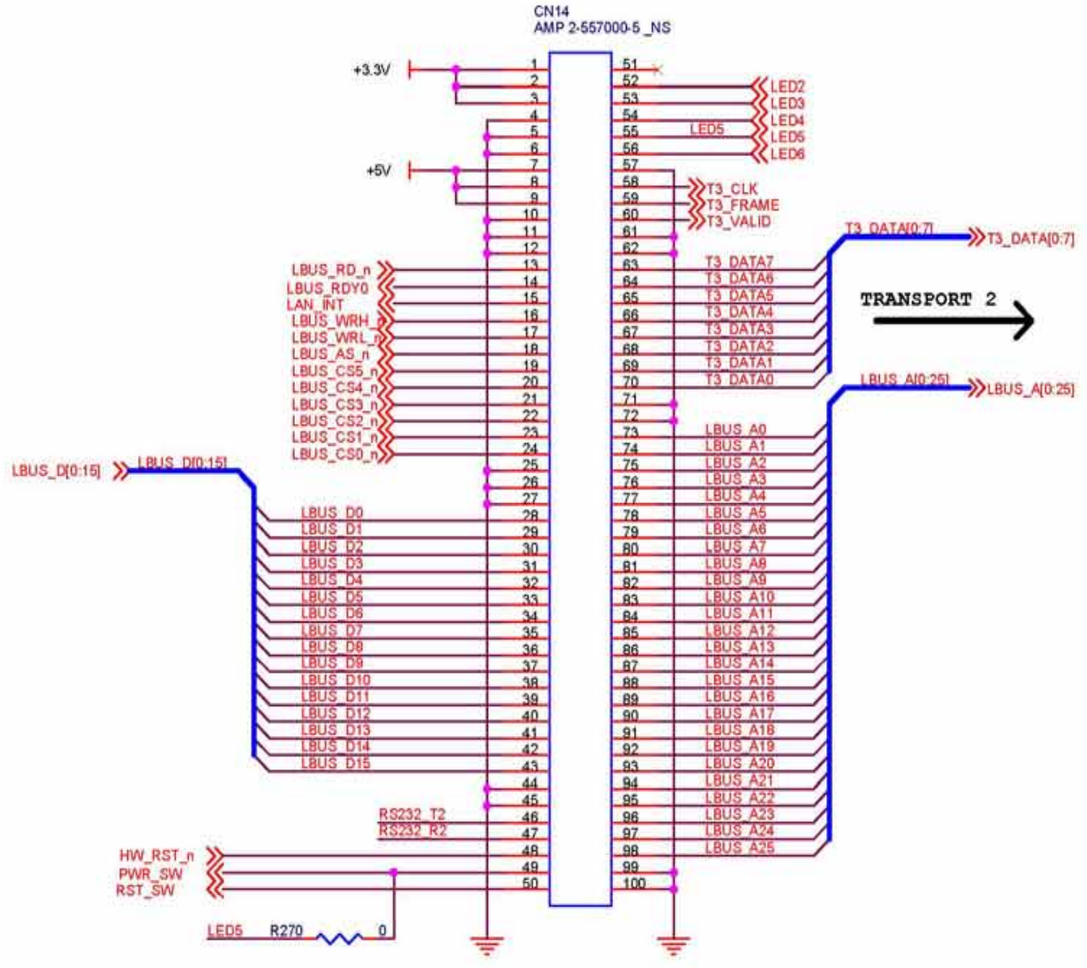
Title: Phobos
Size: B
Document: BOBCAT_D1_Plus.DSN
Sheet 12 of 22
Rev D2
Date: Wednesday, April 13, 2005
Drawn by: O. Marinovsky


U1B
ZR391055
DDR SDRAM 1
S1DATA0
S1DATA1
S1DATA2
S1DATA3
S1DATA4
S1DATA5
S1DATA6
S1DATA7
S1DATA8
S1DATA9
S1DATA10
S1DATA11
S1DATA12
S1DATA13
S1DATA14
S1DATA15
S1DATA16
S1DATA17
S1DATA18
S1DATA19
S1DATA20
S1DATA21
S1DATA22
S1DATA23
S1DATA24
S1DATA25
S1DATA26
S1DATA27
S1DATA28
S1DATA29
S1DATA30
S1DATA31
S1ADR0
S1ADR1
S1ADR2
S1ADR3
S1ADR4
S1ADR5
S1ADR6
S1ADR7
S1ADR8
S1ADR9
S1ADR10
S1ADR11
S1ADR12
S1BS0_n
S1BS1_n
S1DQS0
S1DQS1
S1DQS2
S1DQS3
S1DQM0
S1DQM1
S1DQM2
S1DQM3
S1RAS_n
S1CAS_n
S1WE_n
S1CLK
S1CLK_n
S1CKE_n
S1VREF
ZR391055SH
+2.5V
C123
0.1uF
VREF
C124
0.1uF
Note
All DATA/ADR pins have to be setup as OUTPUT
condition during boot-up.
U1H
ZR391055
SMART CARD
INTERFACES
SC0DET
SC0DATA
SC0AUX1
SC0AUX2
SC0RST
SC0CMDV
SC0CLK
NRSSCLK_GPIO2
SC1DET
SC1DATA
SC1RST
SC1CMDV
SC1CLK
SC0CMDVPP
SC1CMDVPP
HDMI_INT
LAN_INT
AUD_SEL_A
AUD_SEL_B
FSC_LOCK
AUD_SEL_C
SPIEEPROM_WP_n
Video_Input_Select
ACS0
ACS1
ACS2
HD_SYNC_SEL
LED2
AUD_DOWN
FRONT-AV-SEL
To Page5
To Page5
ZR391055SH
U1D
ZR391055
IDE INTERFACE
IDERST_n
IDED7
IDED8
IDED6
IDED9
IDED5
IDED10
IDED4
IDED11
IDED3
IDED12
IDED2
IDED13
IDED1
IDED14
IDED0
IDED15
IDEDRQ
IDEIOW_n
IDEIOR_n
IDERDY
IDEDACK_n
IDEINT
IDEA1
IDEA0
IDEA2
IDECS1_n
IDECS3_n
IDE_RST_n
IDE_D7
IDE_D8
IDE_D6
IDE_D9
IDE_D5
IDE_D10
IDE_D4
IDE_D11
IDE_D3
IDE_D12
IDE_D2
IDE_D13
IDE_D1
IDE_D14
IDE_D0
IDE_D15
IDE_DRQ_n
IDE_IOW_n
IDE_IOR_n
IDE_RDY_n
IDE_DACK_n
IDE_INTR
IDE_A1
IDE_A0
IDE_A2
IDE_CS1_n
IDE_CS3_n
R203
10K
R204
10K
R310 22
R311 82
R312 5.6K
R313 4.7K
+3.3V
R314 82
R315 82
R316 10K
IDE_HSCBL_n
IDE_DASP_n
+5V
Note: Termination resistors should be
located within .4" of the connector.
CN3
IDE_CONN44
TOP VIEW
RESET
GND
D7
D8
D6
D9
D5
D10
D4
D11
D3
D12
D2
D13
D1
D14
D0
D15
GND
KEYED
DMARQ
GND
IOW
GND
DIOR
GND
IORDY
CSEL
DMACK
GND
INTRQ
reserved
A1
PDIAG
A0
A2
CS1
CS3
DASP
GND
+5V
+5V
GND
reserved
2x22 2mm Header
ZR391055SH
Note: Trace lengths for D[0:15] should
be within +/- .5" of the matched trace
lengths for the IDE_RDY- and IDE_IOR-
signals. Line lengths should be less
than 8".
IDE_DASP_n
IDE_LED_n
IDE_HSCBL_n
Reset Logic
U20
Reset Ckt
VCC
/RESET
GND
DS1233A
+3.3V
R215
10K
HW_RST_n
HW_RST_n
C122
560pF
D121
BAV99L
RST_SW
IDE / GPIOs Blocks
Title
Phobos
Size
B
Document
BOBCAT_D1_Plus.DSN
Sheet 13 of 22
Rev D2
Date: Monday, March 28, 2005
Drawn by: O. Marinovsky



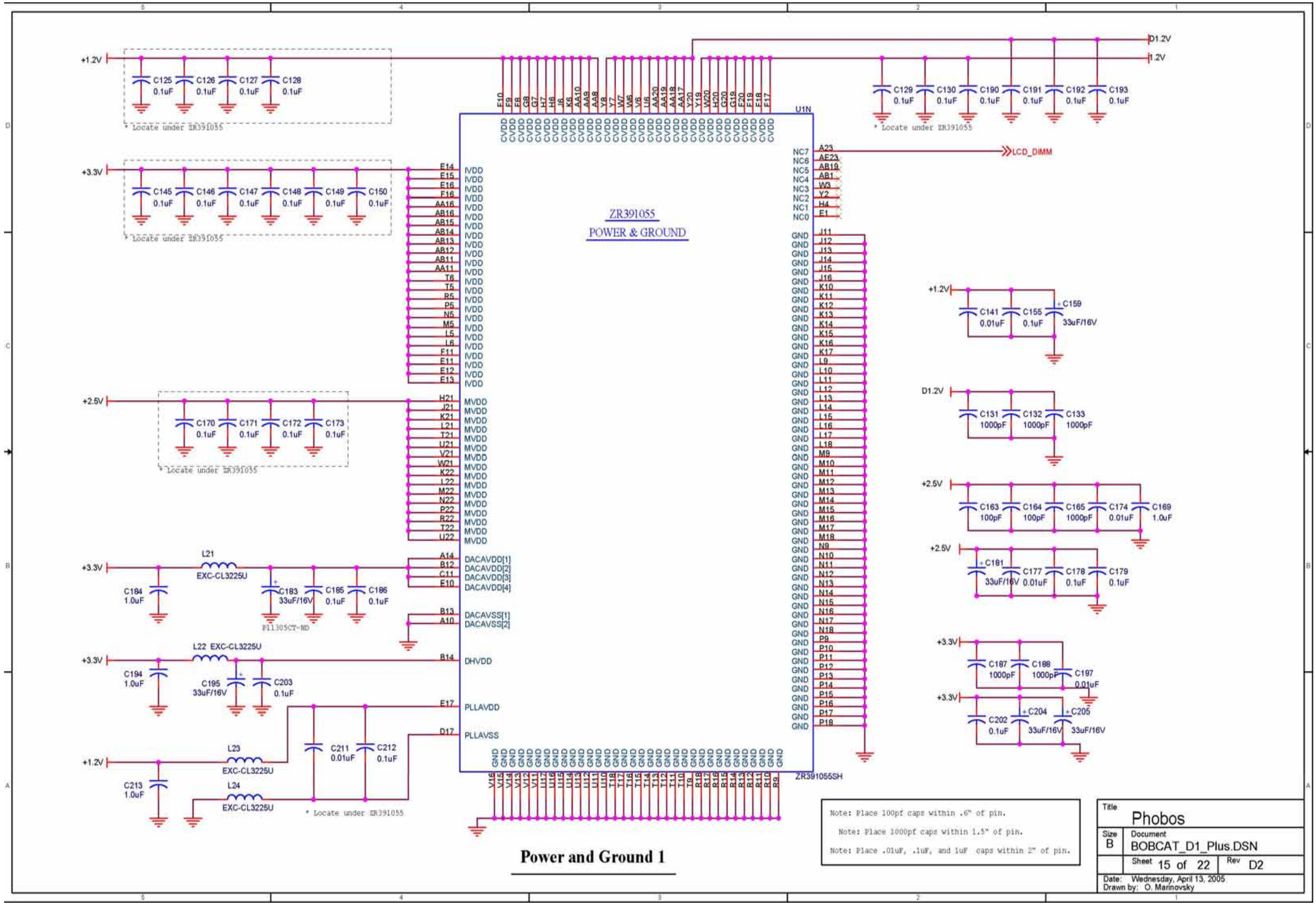


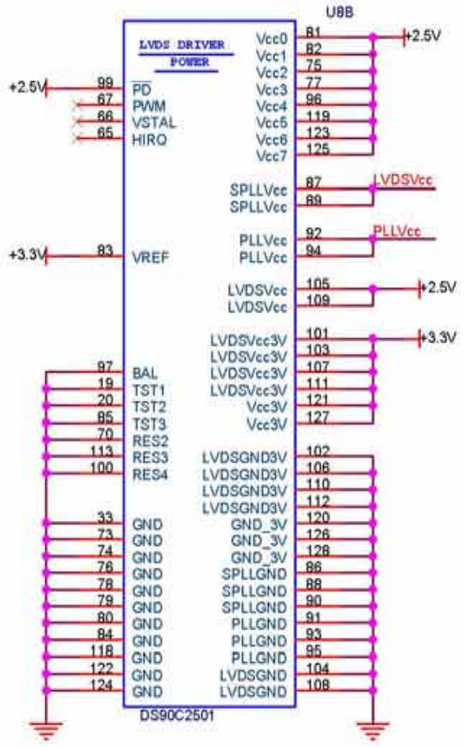


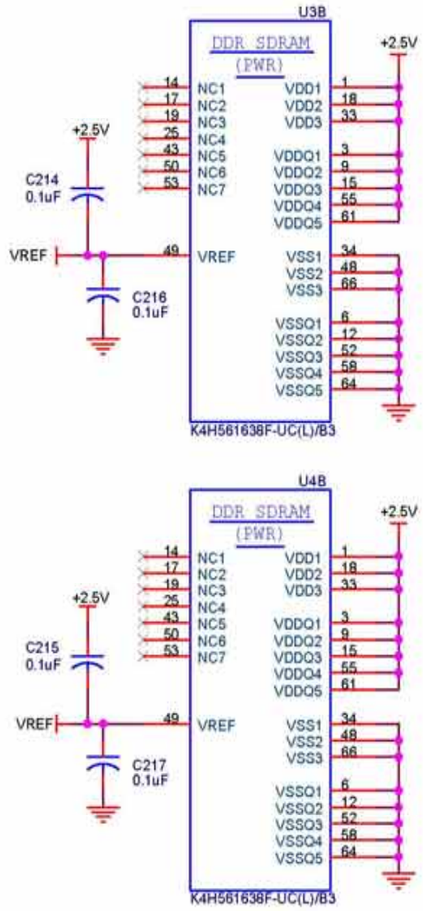


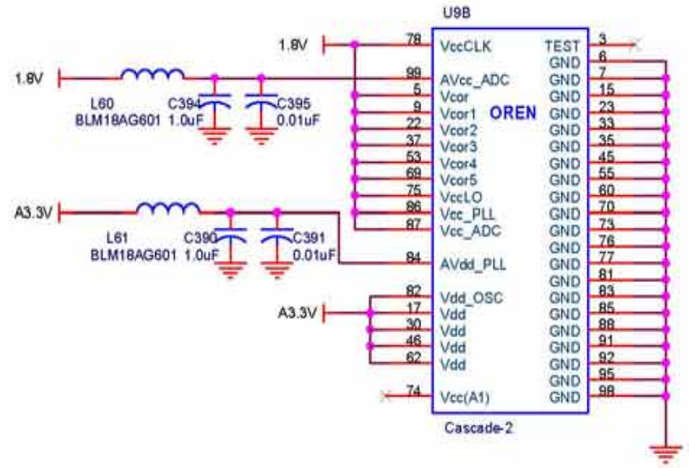
Utility / JTAG Connectors

Title	Phobos
Size B	Document BOBCAT_D1_Plus.DSN
	Sheet 14 of 22 — Rev D2
Date: Wednesday, April 13, 2005	Drawn by: O. Marinovsky

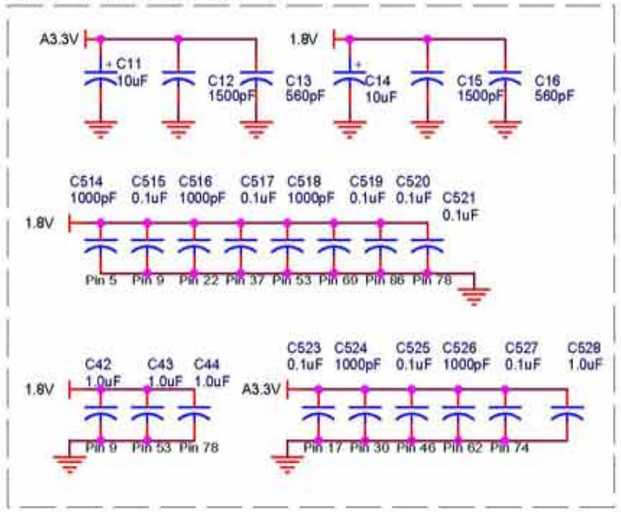

ZR391055
POWER & GROUND
U1N
ZR391055SH
+1.2V
+3.3V
+2.5V
D1.2V
1.2V
LCD_DIMM
* Locate under ZR391055
EXC-CL3225U
P11305CT-ND
Note: Place 100pf caps within .6" of pin.
Note: Place 1000pf caps within 1.5" of pin.
Note: Place .01uF, .1uF, and 1uF caps within 2" of pin.
Power and Ground 1
Title
Phobos
Size
B
Document
BOBCAT_D1_Plus.DSN
Sheet 15 of 22
Rev D2
Date: Wednesday, April 13, 2005
Drawn by: O. Marinovsky



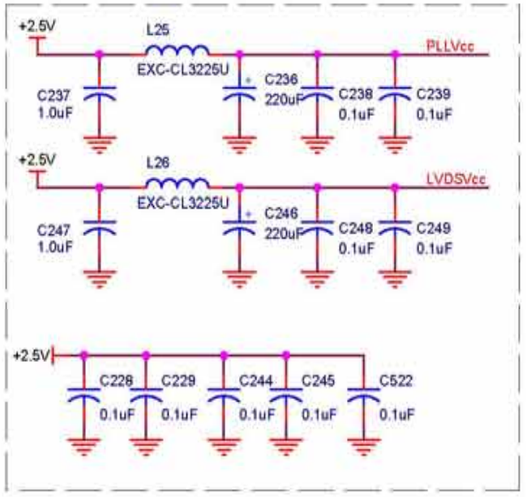




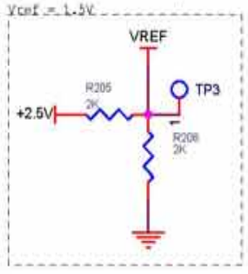
Supply Bypass, Tuner Demodulator



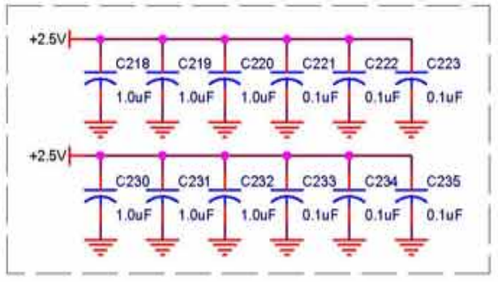
Supply Filters/Bypass, LVDS



Locate between DDR chips.
Vref = 1.5V

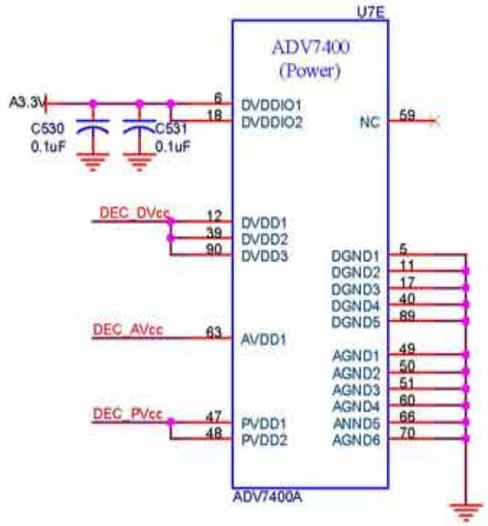


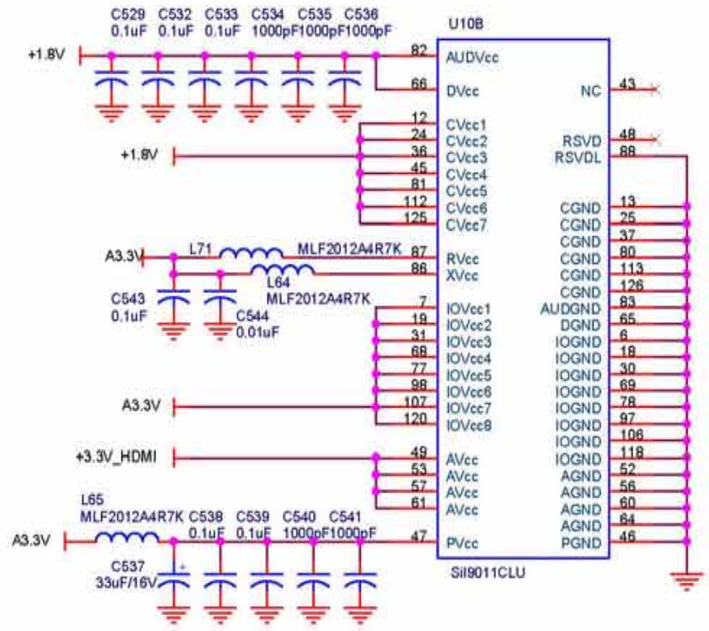
Supply Bypass, DDR S0



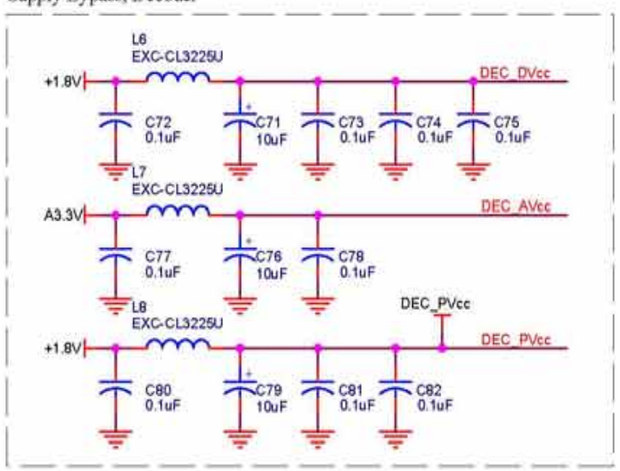
Power and Ground 2

Title	Phobos
Size B	Document BOBCAT_D1_Plus.DSN
Sheet 16 of 22	Rev D2
Date: Wednesday, April 13, 2005	
Drawn by: O. Marinovsky	

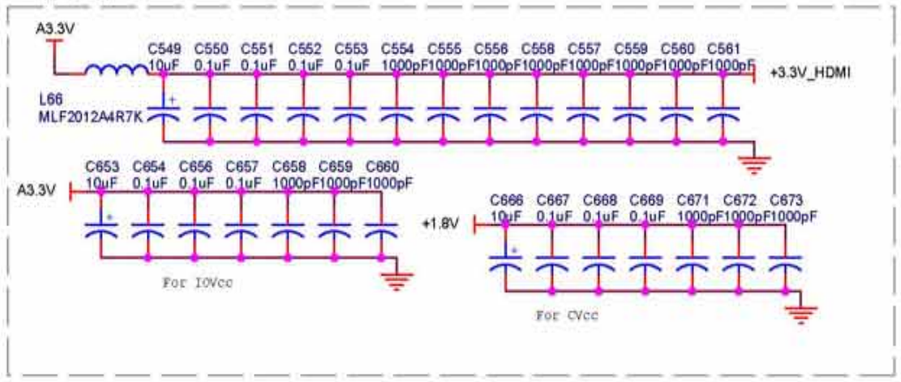




Supply Bypass, Decoder



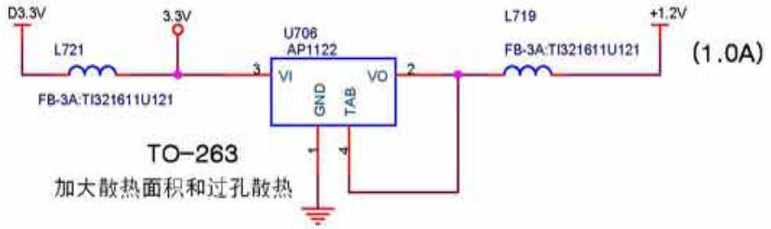
Supply Bypass, HDMI Receiver

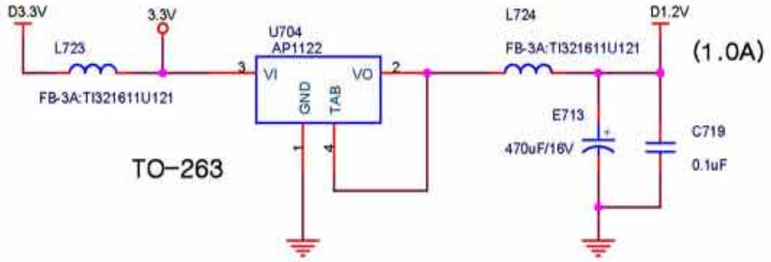


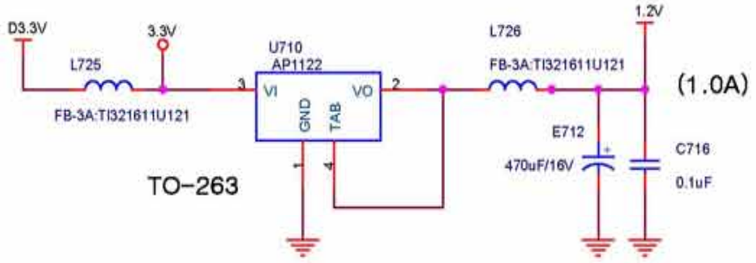
Power & Ground 3

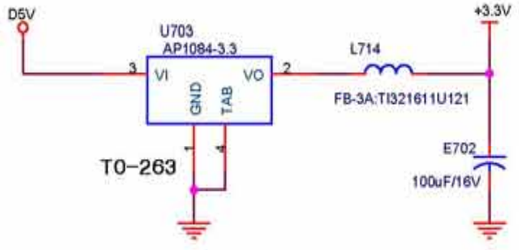
Title	Phobos	
Size B	Document BOBCAT_D1_Plus.DSN	
	Sheet 17 of 22	Rev D2
Date: Wednesday, April 13, 2005	Drawn by: O. Marinovsky	

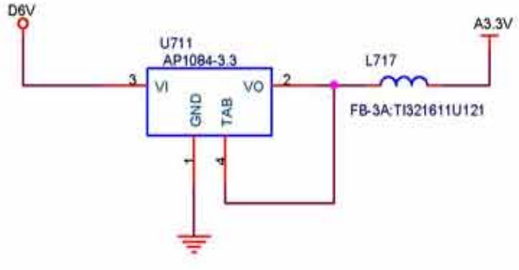
AP1122 1A 1.2V LDO

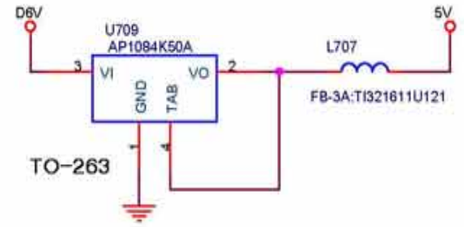


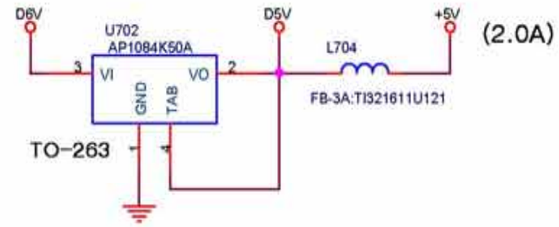


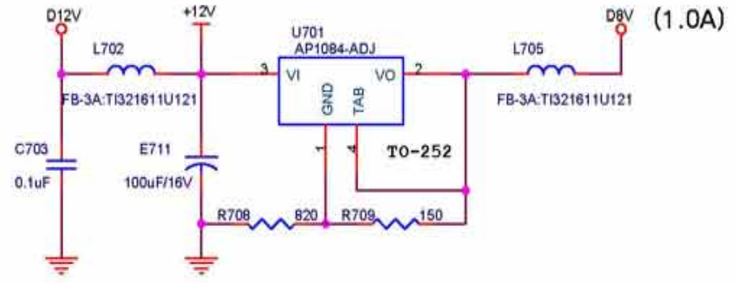


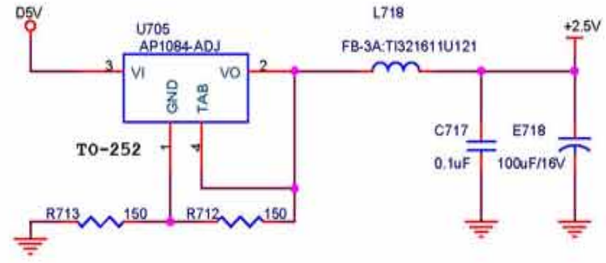








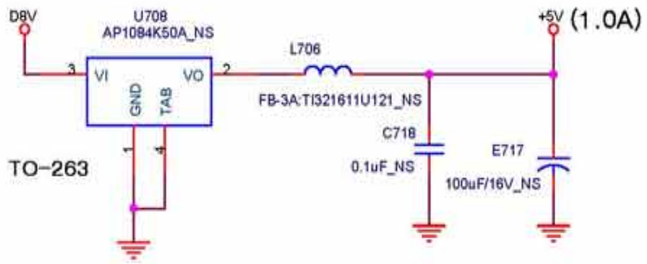


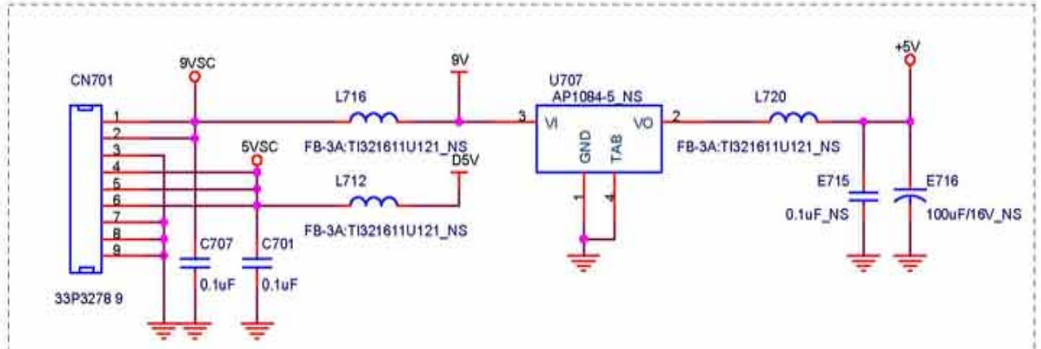


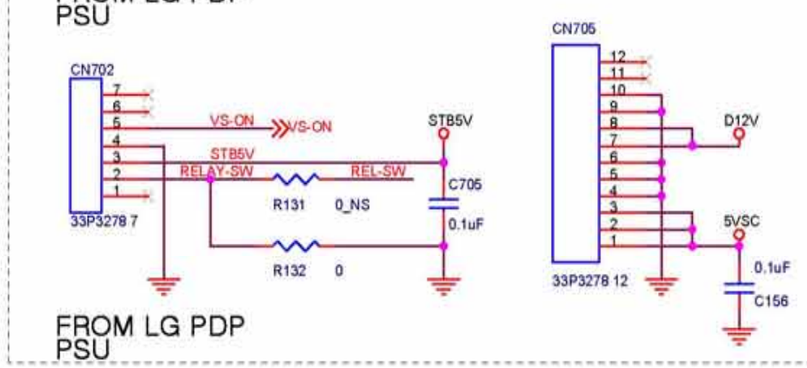
1.2V - 2A (2.8A MAX)
2.5V - 1.6A (2.6A MAX)
3.3V - 1.5A (2.3A MAX)
5.0V - 0.5A (1A MAX)

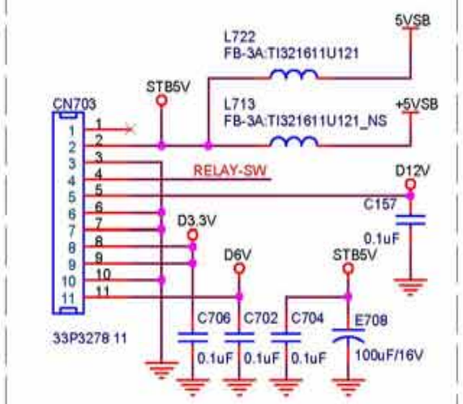
Power & Ground 4

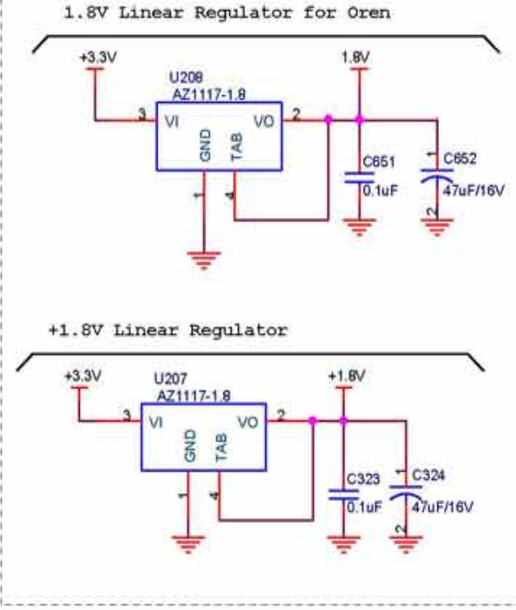
Title: Phobos		
Size: B	Document: BOBCAT_D1_Plus.DSN	
	Sheet 18 of 22	Rev D2
Date: Wednesday, April 13, 2005		
Drawn by: O. Marinovsky		

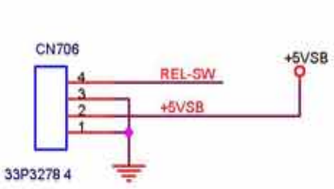


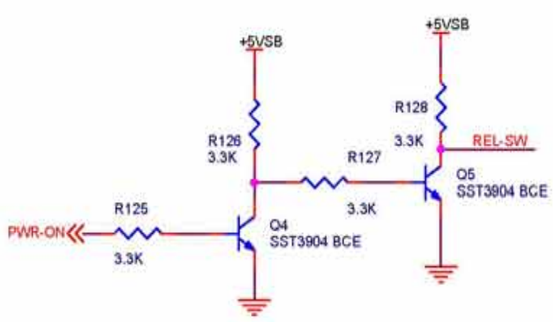


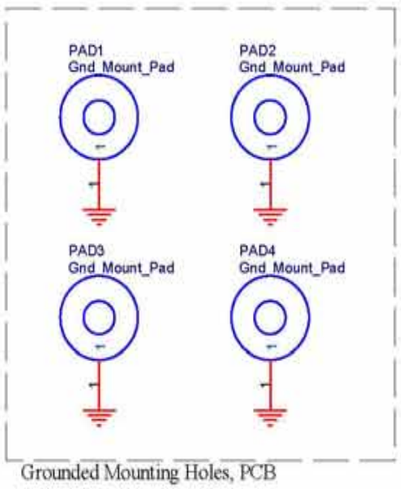


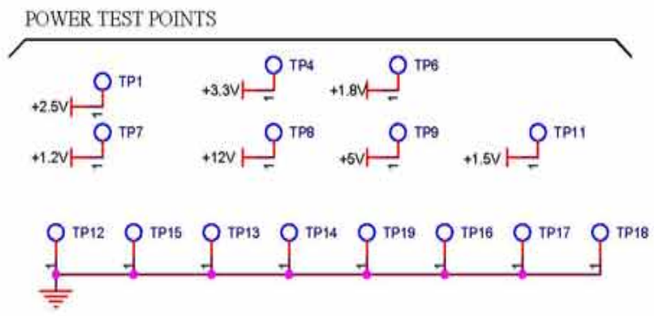






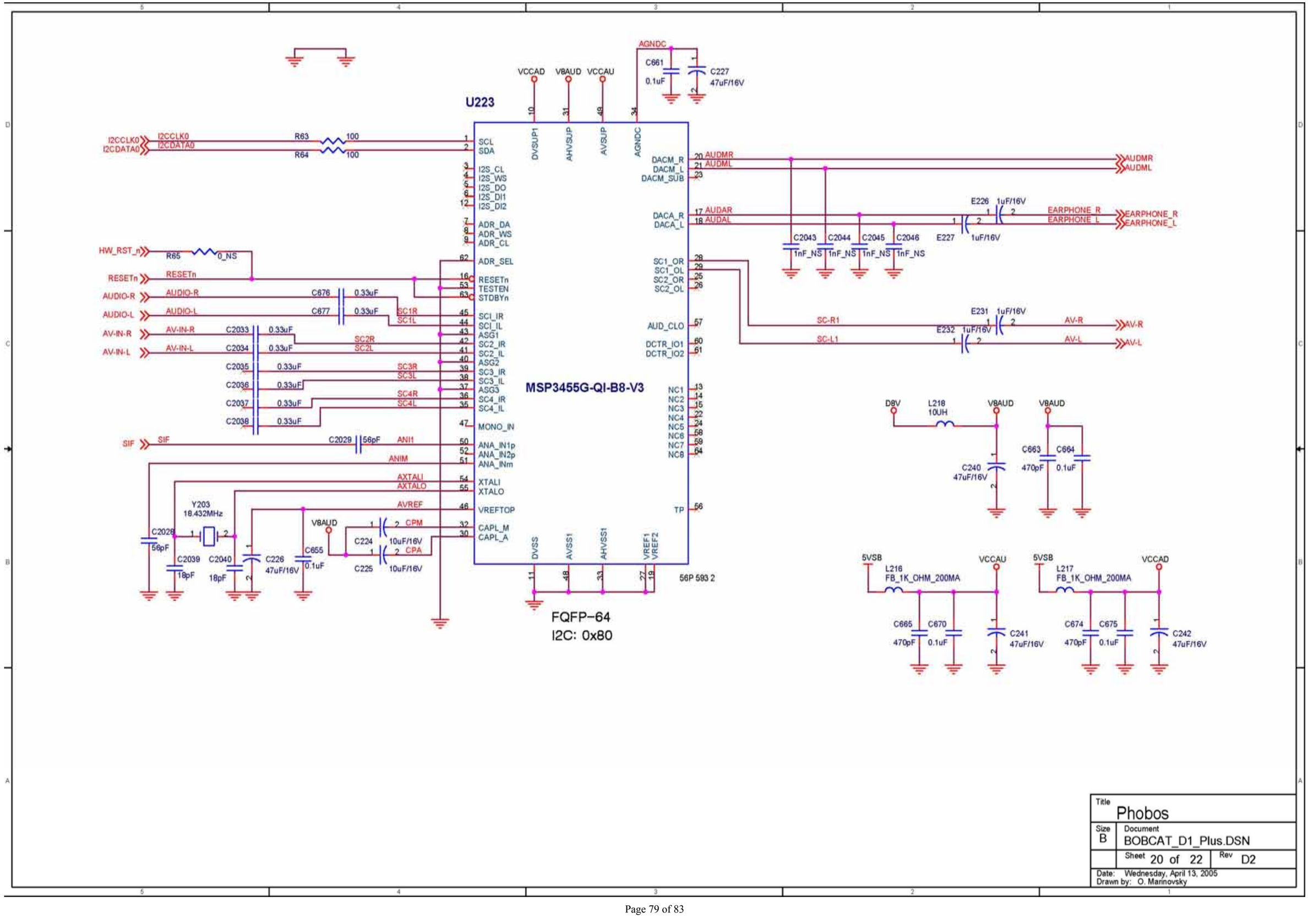


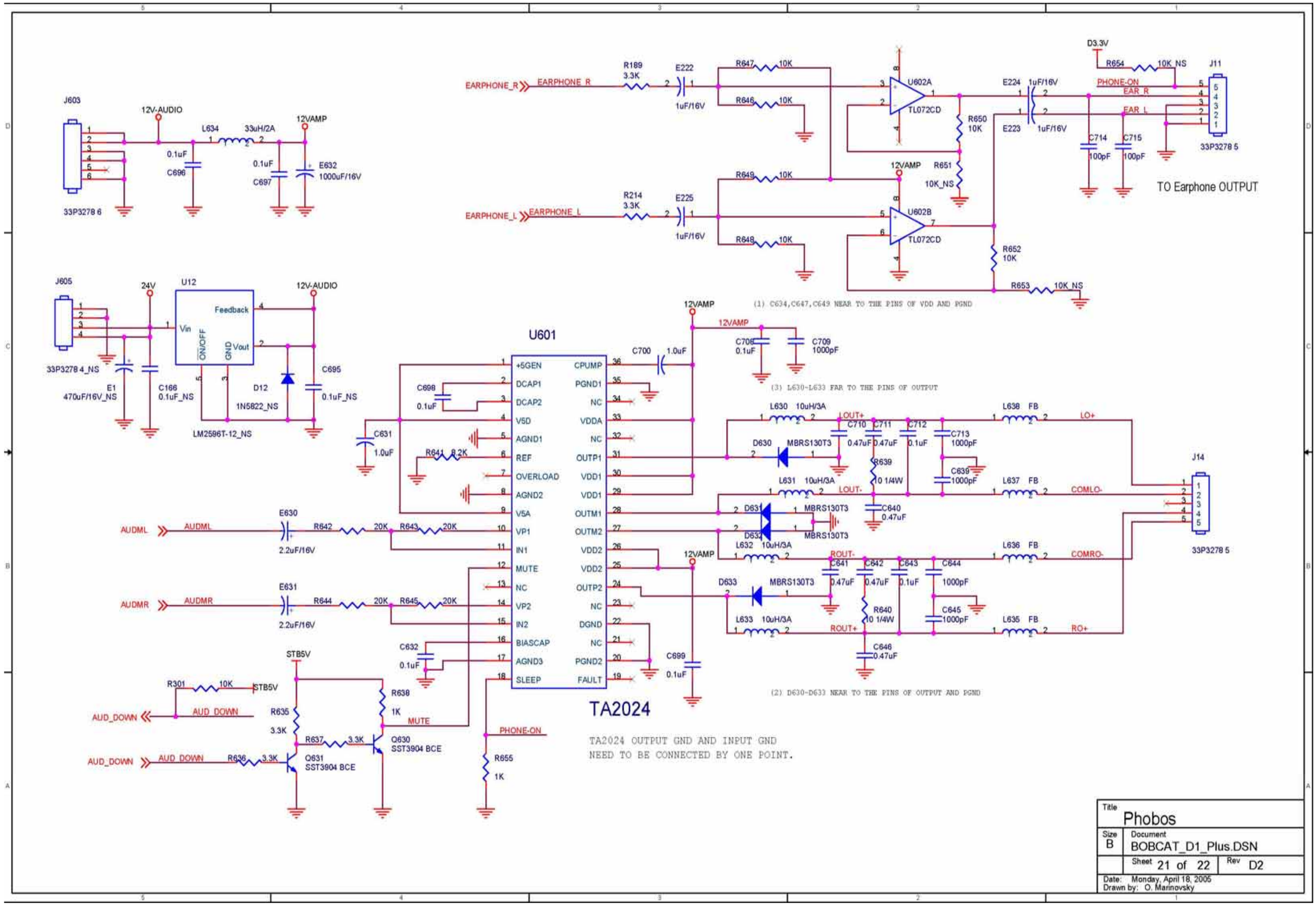




Power & Ground 5

Title	Phobos	
Size B	Document BOBCAT_D1_Plus.DSN	
	Sheet 19 of 22	Rev D2
Date: Wednesday, April 13, 2005		
Drawn by: O. Marinovsky		


U223
MSP3455G-QI-B8-V3
FQFP-64
I2C: 0x80
VCCAD
VBAUD
VCCAU
AGNDC
C661
0.1uF
C227
47uF/16V
I2CCLK0
I2CDATA0
R63
R64
100
HW_RST_n
R65
0_NS
RESETn
AUDIO-R
AUDIO-L
AV-IN-R
AV-IN-L
C676
C677
0.33uF
C2033
C2034
C2035
C2036
C2037
C2038
SC1R
SC1L
SC2R
SC2L
SC3R
SC3L
SC4R
SC4L
SIF
C2029
56pF
ANI1
ANIM
AXTALI
AXTALO
AVREF
Y203
18.432MHz
C2028
C2039
C2040
18pF
C226
47uF/16V
C655
0.1uF
C224
C225
10uF/16V
CPM
CPA
DVSUP1
AHVSUP
AVSUP
AGNDC
SCL
SDA
I2S_CL
I2S_WS
I2S_DO
I2S_DI1
I2S_DI2
ADR_DA
ADR_WS
ADR_CL
ADR_SEL
RESETn
TESTEN
STDBYn
SCI_IR
SCI_IL
ASG1
SC2_IR
SC2_IL
ASG2
SC3_IR
SC3_IL
ASG3
SC4_IR
SC4_IL
MONO_IN
ANA_IN1p
ANA_IN2p
ANA_INm
XTALI
XTALO
VREFTOP
CAPL_M
CAPL_A
DVSS
AVSS1
AHVSS1
VREF1
VREF2
TP
56P 593 2
DACM_R
DACM_L
DACM_SUB
DACA_R
DACA_L
AUDMR
AUDML
AUDAR
AUDAL
SC1_OR
SC1_OL
SC2_OR
SC2_OL
AUD_CLO
DCTR_IO1
DCTR_IO2
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
C2043
C2044
C2045
C2046
1nF_NS
E226
E227
E231
E232
1uF/16V
EARPHONE_R
EARPHONE_L
SC-R1
SC-L1
AV-R
AV-L
D8V
L218
10UH
C240
47uF/16V
C663
470pF
C664
0.1uF
5VSB
L216
FB_1K_OHM_200MA
L217
FB_1K_OHM_200MA
C665
C670
C674
C675
C241
C242
Title
Phobos
Size
B
Document
BOBCAT_D1_Plus.DSN
Sheet 20 of 22
Rev D2
Date: Wednesday, April 13, 2005
Drawn by: O. Marinovsky


J603
12V-AUDIO
L634
33uH/2A
12VAMP
0.1uF
C696
0.1uF
C697
E632
1000uF/16V
33P3278 6
EARPHONE_R
EARPHONE_R
R189
3.3K
E222
1uF/16V
R647
10K
R646
10K
U602A
TL072CD
R650
10K
E224
1uF/16V
E223
1uF/16V
D3.3V
R654
10K_NS
J11
PHONE-ON
EAR_R
EAR_L
C714
100pF
C715
100pF
33P3278 5
TO Earphone OUTPUT
EARPHONE_L
EARPHONE_L
R214
3.3K
E225
1uF/16V
R649
10K
R648
10K
U602B
TL072CD
12VAMP
R651
10K_NS
R652
10K
R653
10K_NS
(1) C634,C647,C649 NEAR TO THE PINS OF VDD AND PGND
J605
24V
U12
Feedback
Vin
ON/OFF
GND
Vout
12V-AUDIO
33P3278 4_NS
E1
470uF/16V_NS
C166
0.1uF_NS
D12
1N5822_NS
C695
0.1uF_NS
LM2596T-12_NS
U601
12VAMP
C700
1.0uF
C705
0.1uF
C709
1000pF
(3) L630-L633 FAR TO THE PINS OF OUTPUT
+5GEN
DCAP1
DCAP2
V5D
AGND1
REF
OVERLOAD
AGND2
V5A
VP1
IN1
MUTE
NC
VP2
IN2
BIASCAP
AGND3
SLEEP
CPUMP
PGND1
NC
VDDA
NC
OUTP1
VDD1
VDD1
OUTM1
VDD2
VDD2
OUTP2
NC
DGND
NC
PGND2
FAULT
C698
0.1uF
C631
1.0uF
R641 8.2K
C632
0.1uF
C699
0.1uF
L630 10uH/3A
L631 10uH/3A
L632 10uH/3A
L633 10uH/3A
L638 FB
L637 FB
L636 FB
L635 FB
OUT+
LOUT-
ROUT-
ROUT+
LO+
COMLO-
COMRO-
RO+
C710
0.47uF
C711
0.47uF
C712
0.1uF
C713
1000pF
C639
1000pF
C644
1000pF
C645
1000pF
C640
0.47uF
C641
0.47uF
C642
0.47uF
C643
0.1uF
C646
0.47uF
R639
10 1/4W
R640
10 1/4W
D630
MBRS130T3
D631
MBRS130T3
D632
MBRS130T3
D633
MBRS130T3
J14
33P3278 5
E630
AUDML
AUDML
R642
20K
R643
20K
2.2uF/16V
E631
AUDMR
AUDMR
R644
20K
R645
20K
2.2uF/16V
STB5V
R301
10K
STB5V
AUD_DOWN
AUD_DOWN
R635
3.3K
R637
3.3K
Q630
SST3904 BCE
AUD_DOWN
AUD_DOWN
R636
3.3K
Q631
SST3904 BCE
R638
1K
MUTE
PHONE-ON
R655
1K
TA2024
TA2024 OUTPUT GND AND INPUT GND
NEED TO BE CONNECTED BY ONE POINT.
(2) D630-D633 NEAR TO THE PINS OF OUTPUT AND PGND
Title
Phobos
Size
B
Document
BOBCAT_D1_Plus.DSN
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Rev D2
Date: Monday, April 18, 2005
Drawn by: O. Marinovsky

GPIO Pin Table

Signal	ZR391055 GPIO #	Function	Setting
LCD_ON	0	LCD backlight ON/OFF control.	Active high.
NAND_GPIO1_n	1	Allow to boot-up from NAND FLASH	Active low.
Video_Input_Select	2	Composite - Y/C Video Input recognition.	1 = Composite, 0 = Y/C
WP~	3	NAND FLASH WR protection	1 = WR Enable, 0 = protected.
CH +	4	Tuner control / Setup errow	Active low.
CH -	5	Tuner control / Setup errow	Active low.
VOL +	6	VOL control / Setup errow	Active low.
VOL -	7	VOL control / Setup errow	Active low.
AUD_DOWN	11	AUD_DOWN MUTE	
AUD_SEL_A	12	AUDIO IN Select	(see table p.05)
AUD_SEL_B	13	AUDIO IN Select	(see table p.05)
AUD_SEL_C	14	AUDIO IN Select	(see table p.05)
CVmix_SEL	104	Analog video composite summer	
HD_DOWN	107	Head Phone MUTE	Active low
ACLK_SEL0	108	ACLK select source - HDMI/CLK GEN	Active low.
ACLK_SEL1	109	ACLK select source - HDMI/CLK GEN	Active low.
FMS_SEL	110	RGB out filter select HD/SD	
HDMI_SCDT	112	HDMI Signal Detect	Active high.
TV_VIDEO	113	VIDEIO IN Select / FP SW	Active low.
IDE_HSCBL_n	119		Active low.
AIN_INT_n	120	Analog Decoder IC Int.	Active low.
HD_SEL	121	2 COMPONENT SIGNAL SW	(see table p.07)
CEC	122	HDMI control	
SLEEP_MODE_n	123	LOW PWR mode control	Active low.
HDMI_VSYNC	125	SYNC signal control from HDMI sourse.	
SPIEEPROM_WP_n	154	SPI EEPROM Wright protection.	Active low.
LAN_INT	155	Ethernet IC Int.	Active high.
HDMI_INT	156	HDMI IC Int.	Active high.
FSC_LOCK	157	Subcarrier Frequency Lock	
LCD_PWM	158	LCD PWM Control.	
ACS0	161	Audio Clock Freq. Sel bit 0 (Main)	(see table p11)
ACS1	160	Audio Clock Freq. Sel bit 1 (Main)	(see table p11)
ACS2	162	Audio Clock Freq. Sel bit 2 (Main)	(see table p11)
HD_SYNC_SEL	163	HD_SYNC_SEL	
LED2	159	LED D2 Control	1 = off, 0 = lit
LED3	166	LED D3 Control	1 = off, 0 = lit
LED4	167	LED D4 Control	1 = off, 0 = lit
LED5	168	LED D5 Control	1 = off, 0 = lit
LED6	169	LED D6 Control	1 = off, 0 = lit
MENU	184	SEL / FP SW	Active low.

DS90C2501 GPIO#	Function	Setting
0	LVDS Control	
1	COLOR Function	Active low.
2	DUAL Function	Active high.

GPOIs Table

Title: Phobos			
Size: B	Document: BOBCAT_D1_Plus.DSN		
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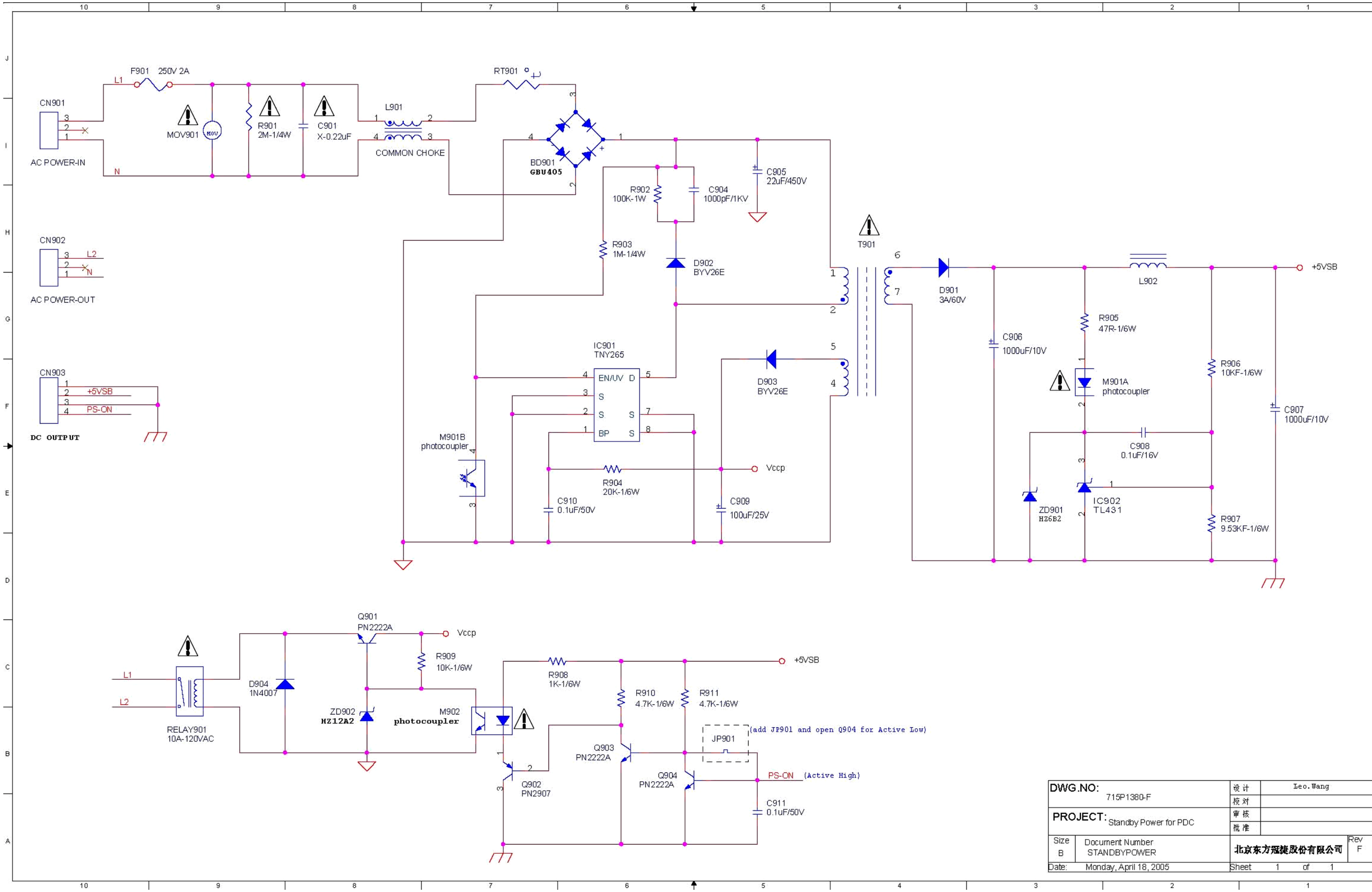
CN901
AC POWER-IN
F901 250V 2A
L1
N
MOV901
R901 2M-1/4W
C901 X-0.22uF
L901
COMMON CHOKE
RT901
BD901 GBU405
C905 22uF/450V
R902 100K-1W
C904 1000pF/1KV
R903 1M-1/4W
D902 BYV26E
T901
D901 3A/60V
L902
+5VSB
CN902
AC POWER-OUT
L2
N
IC901 TNY265
EN/UV
BP
D903 BYV26E
C906 1000uF/10V
R905 47R-1/6W
M901A photocoupler
R906 10KF-1/6W
C907 1000uF/10V
C908 0.1uF/16V
ZD901 HZ6B2
IC902 TL431
R907 9.53KF-1/6W
CN903
+5VSB
PS-ON
DC OUTPUT
M901B photocoupler
R904 20K-1/6W
C910 0.1uF/50V
C909 100uF/25V
Vccp
Q901 PN2222A
R909 10K-1/6W
D904 1N4007
ZD902 HZ12A2
M902 photocoupler
R908 1K-1/6W
R910 4.7K-1/6W
R911 4.7K-1/6W
JP901
(add JP901 and open Q904 for Active Low)
Q903 PN2222A
Q904 PN2222A
Q902 PN2907
PS-ON (Active High)
C911 0.1uF/50V
RELAY901 10A-120VAC
DWG.NO: 715P1380-F
PROJECT: Standby Power for PDC
设计 Leo.Wang
校对
审核
批准
Size B
Document Number STANDBYPOWER
北京东方冠捷股份有限公司
Rev F
Date: Monday, April 18, 2005
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